

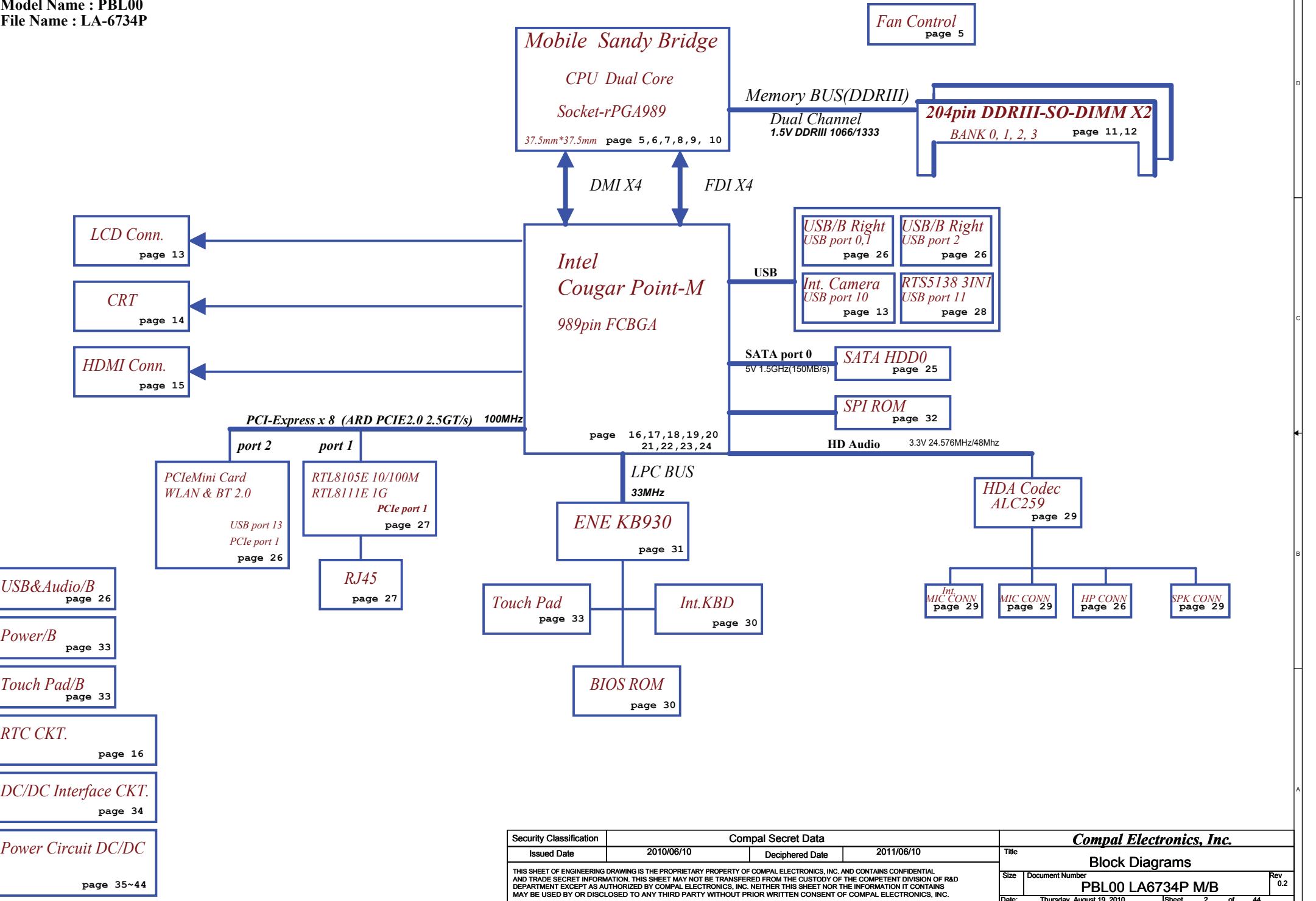
Compal Confidential

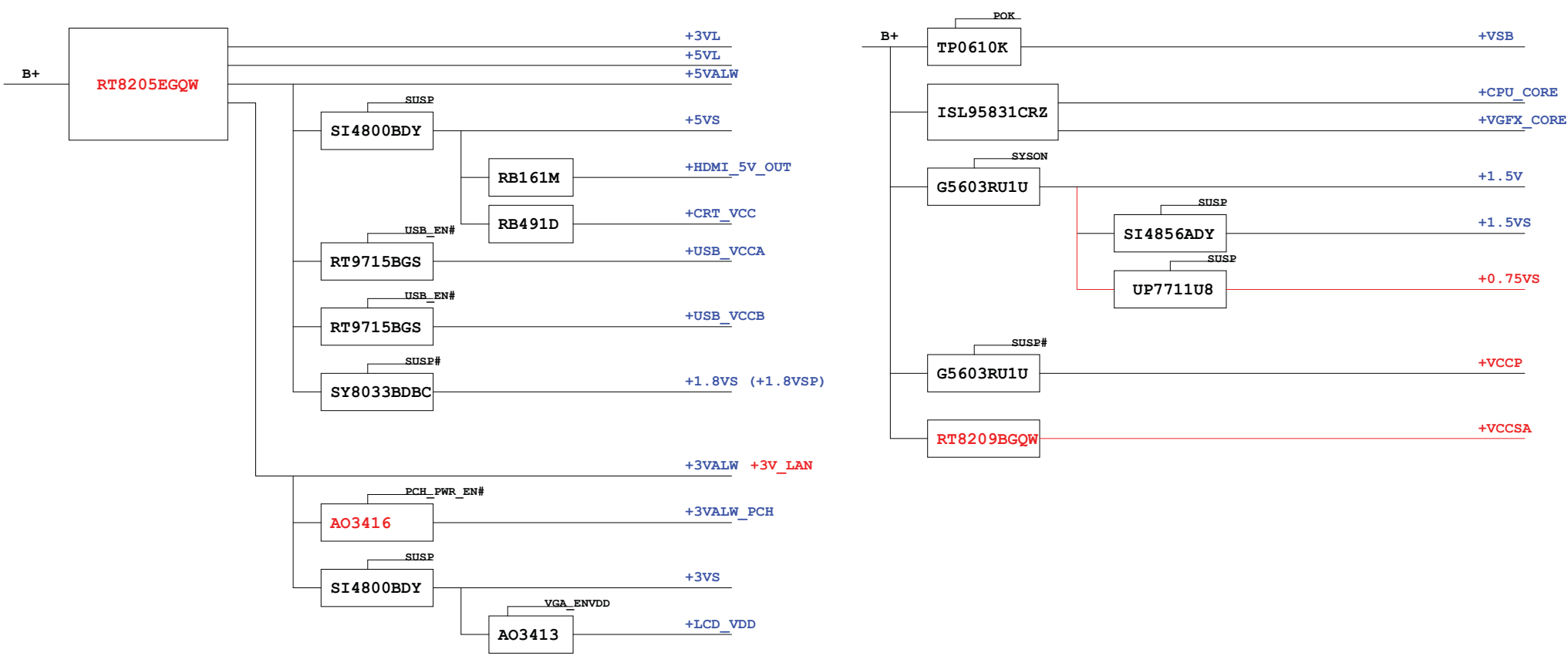
PBL00

LA-6734P REV 0.2 Schematic

Intel Sandy Bridge/Cougar Point (UMA)
2010-10-28 Rev. 0.2

| | | | | | |
|---|------------|--------------------|------------|---------------------------|------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2010/06/10 | Deciphered Date | 2011/06/10 | Title Cover Page | |
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| Date: Thursday, October 28, 2010 | | Sheet 1 of 44 | | | |





Voltage Rails

| Power Plane | Description | S1 | S3 | S5 |
|---|---|-----|-----|-----|
| VIN | Adapter power supply (19V) | N/A | N/A | N/A |
| BATT+ | Battery power supply (12.6V) | N/A | N/A | N/A |
| B+ | AC or battery power rail for power circuit. | N/A | N/A | N/A |
| +CPU_CORE | Core voltage for CPU | ON | OFF | OFF |
| +VGA_CORE | Core voltage for GPU | ON | OFF | OFF |
| +VGFX_CORE | Core voltage for UMA graphic | ON | OFF | OFF |
| +0.75VS | +0.75VP to +0.75VS switched power rail for DDR terminator | ON | OFF | OFF |
| +1.0VSDGPU | +1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU | ON | OFF | OFF |
| +VCCP | +1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU | ON | OFF | OFF |
| +1.05VS_PCH | +1.05VS_VCCP to +1.05VS_PCH power for PCH | ON | OFF | OFF |
| +1.5V | +1.5VP to +1.5V power rail for DDRIII | ON | ON | OFF |
| +1.5VS | +1.5V to +1.5VS switched power rail | ON | OFF | OFF |
| +1.5VSDGPU | +1.5VS to +1.5VSDGPU switched power rail for GPU | ON | OFF | OFF |
| +1.8VS | (+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU | ON | OFF | OFF |
| +3VALW | +3VALW always on power rail | ON | ON | ON* |
| +3VALW_EC | +3VALW always to KBC | ON | ON | ON* |
| +3V_LAN | +3VALW to +3V_LAN power rail for LAN | ON | ON | ON* |
| +3VALW_PCH | +3VALW to +3VALW_PCH power rail for PCH (Short Jumper) | ON | ON | ON* |
| +3VS | +3VALW to +3VS power rail | ON | OFF | OFF |
| +5VALW | +5VALWP to +5VALW power rail | ON | ON | ON* |
| +5VALW_PCH | +5VALW to +5VALW_PCH power rail for PCH (Short resister) | ON | ON | ON* |
| +5VS | +5VALW to +5VS switched power rail | ON | OFF | OFF |
| +VSB | +VSBP to +VSB always on power rail for sequence control | ON | ON | ON* |
| +RTCVCC | RTC power | ON | ON | ON |
| Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF. | | | | |

| STATE \ SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V | +VS | Clock |
|-----------------------|---------|---------|---------|---------|-------|-----|-----|-------|
| Full ON | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S1 (Power On Suspend) | LOW | HIGH | HIGH | HIGH | ON | ON | ON | LOW |
| S3 (Suspend to RAM) | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | LOW | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF |

EC SM Bus1 address

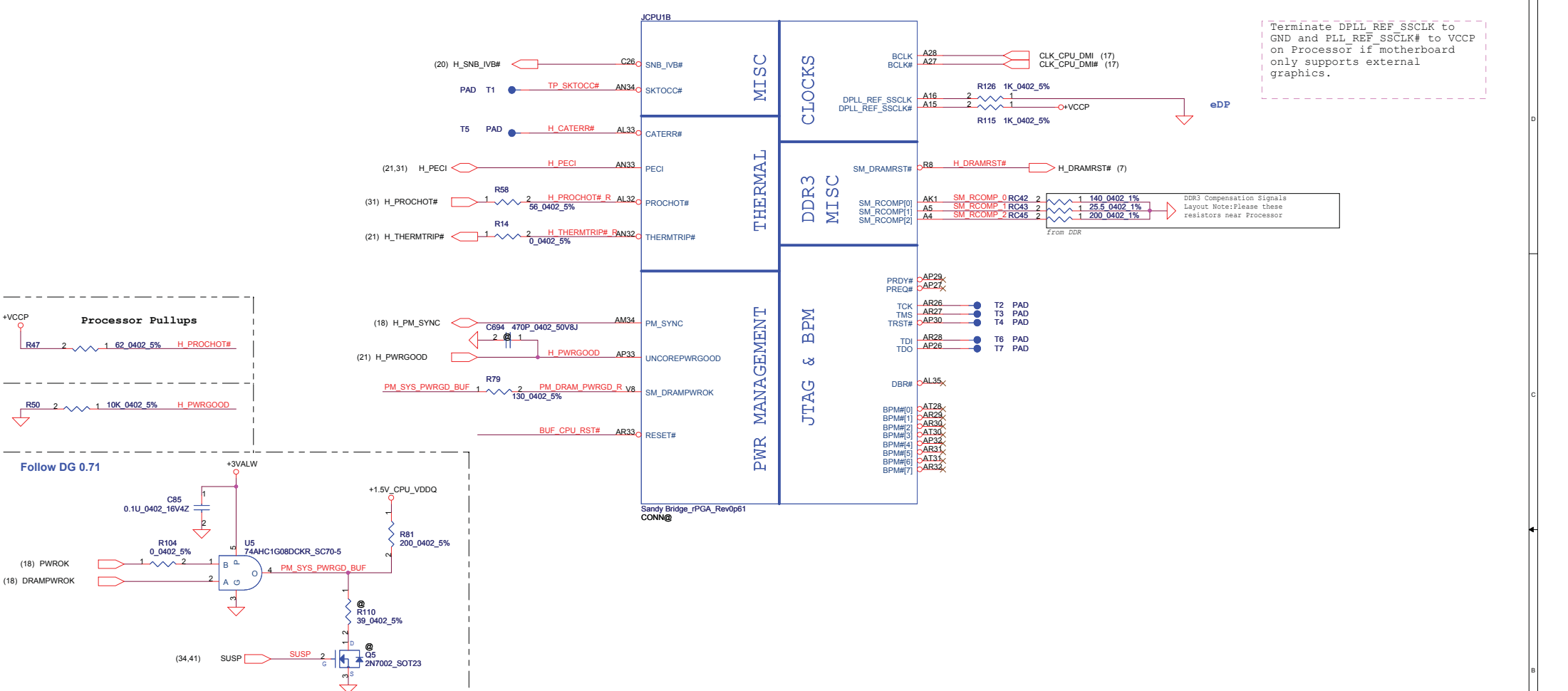
| Power | Device | Address | Power | Device | Address |
|--------|---------------|-------------|--------|--------------------|---------|
| +3VALW | EC KB930 | | +3VS | EC KB930 | |
| +3VL | Smart Battery | 0001 011x b | +3VS | GPU Thermal Sensor | |
| | | | +3VALW | PCH | |

EC SM Bus2 address

PCH SM Bus address

| Power | Device | Address |
|--------|-----------------|-------------|
| +3VALW | PCH | |
| +3VS | Clock Generator | 1101 001x b |
| +3VS | DDR DIMMA | 1001 000x b |
| +3VS | DDR DIMMb | 1001 010x b |
| +3VS | Slot#1--WLAN | |

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| | | | | Date: Wednesday, August 18, 2010 | Sheet 4 of 44 | |



Terminate DPLL_REF_SSCLK to GND and PLL_REF_SSCLK# to VCCP on Processor if motherboard only supports external graphics.

DDR3 Compensation Signals
Layout Note: Please these resistors near Processor
From DDR

| | | | | | |
|---|------------|--------------------|------------|-------------------------------------|----------------------------|
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| | | | | Date | Thursday, October 28, 2010 |
| | | | | Sheet | 5 of 44 |
| | | | | Rev | 0.2 |

(11) DDR_A_D[0..63]

JCPU1C

DDR A D0 C5
DDR A D1 D5
DDR A D2 D3
DDR A D3 D2
DDR A D4 D6
DDR A D5 C6
DDR A D6 C2
DDR A D7 C3
DDR A D8 F10
DDR A D9 F8
DDR A D10 G10
DDR A D11 G9
DDR A D12 F9
DDR A D13 F7
DDR A D14 G8
DDR A D15 G7
DDR A D16 K4
DDR A D17 K5
DDR A D18 K1
DDR A D19 J1
DDR A D20 J5
DDR A D21 J4
DDR A D22 J2
DDR A D23 K2
DDR A D24 M6
DDR A D25 N10
DDR A D26 N8
DDR A D27 N7
DDR A D28 M10
DDR A D29 M9
DDR A D30 N9
DDR A D31 M7
DDR A D32 AG5
DDR A D33 AG5
DDR A D34 AK6
DDR A D35 AK5
DDR A D36 AK5
DDR A D37 AH6
DDR A D38 AJ5
DDR A D39 AJ6
DDR A D40 AK6
DDR A D41 AK6
DDR A D42 AJ9
DDR A D43 AK9
DDR A D44 AH8
DDR A D45 AH9
DDR A D46 AL9
DDR A D47 AL8
DDR A D48 AP11
DDR A D49 AN11
DDR A D50 AL12
DDR A D51 AM12
DDR A D52 AM11
DDR A D53 AL11
DDR A D54 AP12
DDR A D55 AN12
DDR A D56 AJ14
DDR A D57 AH14
DDR A D58 AL15
DDR A D59 AK15
DDR A D60 AL14
DDR A D61 AK14
DDR A D62 AJ15
DDR A D63 AH15

DDR SYSTEM MEMORY A

SA_CLK[0]
SA_CLK#0
SA_CKE[0]

SA_CLK[1]
SA_CLK#1
SA_CKE[1]

SA_CLK[2]
SA_CLK#2
SA_CKE[2]

SA_CLK[3]
SA_CLK#3
SA_CKE[3]

SA_CS#0
SA_CS#1
SA_CS#2
SA_CS#3

SA_ODT[0]
SA_ODT[1]
SA_ODT[2]
SA_ODT[3]

SA_DQS#0
SA_DQS#1
SA_DQS#2
SA_DQS#3
SA_DQS#4
SA_DQS#5
SA_DQS#6
SA_DQS#7

SA_DQS0
SA_DQS1
SA_DQS2
SA_DQS3
SA_DQS4
SA_DQS5
SA_DQS6
SA_DQS7

SA_MA[0]
SA_MA[1]
SA_MA[2]
SA_MA[3]
SA_MA[4]
SA_MA[5]
SA_MA[6]
SA_MA[7]
SA_MA[8]
SA_MA[9]
SA_MA[10]
SA_MA[11]
SA_MA[12]
SA_MA[13]
SA_MA[14]
SA_MA[15]

AB6
AA6
V9

AA5
AB5
V10

AB4
AA4
V9

AB3
AA3
V10

AK3
AL3
AG1
AH1

AH3
AG3
AG2
AH2

C4
G6
J3
M6
AL6
AM8
AR12
AM15

D4
F6
K3
N6
AL5
AM9
AR11
AM14

AD10
W1
W2
W7
V3
V2
W3
W6
V1
W5
AD8
V4
W4
V5
V7

SA_BS[0]
SA_BS[1]
SA_BS[2]

SA_CAS#
SA_RAS#
SA_WE#

Sandy Bridge_PGA_Rev0p61

CONN@

(12) DDR_B_D[0..63]

JCPU1D

DDR B D0 C9
DDR B D1 A7
DDR B D2 C10
DDR B D3 C8
DDR B D4 A9
DDR B D5 A8
DDR B D6 D8
DDR B D7 D8
DDR B D8 G4
DDR B D9 F4
DDR B D10 F1
DDR B D11 G5
DDR B D12 G5
DDR B D13 F5
DDR B D14 F2
DDR B D15 G2
DDR B D16 J7
DDR B D17 J8
DDR B D18 K10
DDR B D19 K9
DDR B D20 J8
DDR B D21 J10
DDR B D22 K8
DDR B D23 K7
DDR B D24 M6
DDR B D25 N4
DDR B D26 N2
DDR B D27 M1
DDR B D28 M4
DDR B D29 N5
DDR B D30 M2
DDR B D31 M1
DDR B D32 AM5
DDR B D33 AM6
DDR B D34 AR3
DDR B D35 AP3
DDR B D36 AN3
DDR B D37 AN2
DDR B D38 AN1
DDR B D39 AP2
DDR B D40 AP5
DDR B D41 AN9
DDR B D42 AT5
DDR B D43 AT6
DDR B D44 AP6
DDR B D45 AN8
DDR B D46 AR6
DDR B D47 AR5
DDR B D48 AR9
DDR B D49 AJ11
DDR B D50 AT8
DDR B D51 AT9
DDR B D52 AH11
DDR B D53 AR8
DDR B D54 AJ12
DDR B D55 AH12
DDR B D56 AT11
DDR B D57 AN14
DDR B D58 AR14
DDR B D59 AT14
DDR B D60 AT12
DDR B D61 AN15
DDR B D62 AR15
DDR B D63 AT15

DDR SYSTEM MEMORY B

SB_CLK[0]
SB_CLK#0
SB_CKE[0]

SB_CLK[1]
SB_CLK#1
SB_CKE[1]

SB_CLK[2]
SB_CLK#2
SB_CKE[2]

SB_CLK[3]
SB_CLK#3
SB_CKE[3]

SB_CS#0
SB_CS#1
SB_CS#2
SB_CS#3

SB_ODT[0]
SB_ODT[1]
SB_ODT[2]
SB_ODT[3]

SB_DQS#0
SB_DQS#1
SB_DQS#2
SB_DQS#3
SB_DQS#4
SB_DQS#5
SB_DQS#6
SB_DQS#7

SB_DQS0
SB_DQS1
SB_DQS2
SB_DQS3
SB_DQS4
SB_DQS5
SB_DQS6
SB_DQS7

SB_MA[0]
SB_MA[1]
SB_MA[2]
SB_MA[3]
SB_MA[4]
SB_MA[5]
SB_MA[6]
SB_MA[7]
SB_MA[8]
SB_MA[9]
SB_MA[10]
SB_MA[11]
SB_MA[12]
SB_MA[13]
SB_MA[14]
SB_MA[15]

SB_BS[0]
SB_BS[1]
SB_BS[2]

SB_CAS#
SB_RAS#
SB_WE#

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CONN@

(11) DDR_A_BS0
(11) DDR_A_BS1
(11) DDR_A_BS2

(11) DDR_A_CAS#
(11) DDR_A_RAS#
(11) DDR_A_WE#

Sandy Bridge_PGA_Rev0p61

CONN@

(12) DDR_B_BS0
(12) DDR_B_BS1
(12) DDR_B_BS2

(12) DDR_B_CAS#
(12) DDR_B_RAS#
(12) DDR_B_WE#

(12) DDR_B_BS0
(12) DDR_B_BS1
(12) DDR_B_BS2

(12) DDR_B_CAS#
(12) DDR_B_RAS#
(12) DDR_B_WE#

Sandy Bridge_PGA_Rev0p61

CONN@

(5) H_DRAMRST#

H_DRAMRST#

Q6
BSS138_NL_SOT23-3

DDR3_DRAMRST# R

SM_DRAMRST# (11,12)

(17) DRAMRST_CNTRL_PCH

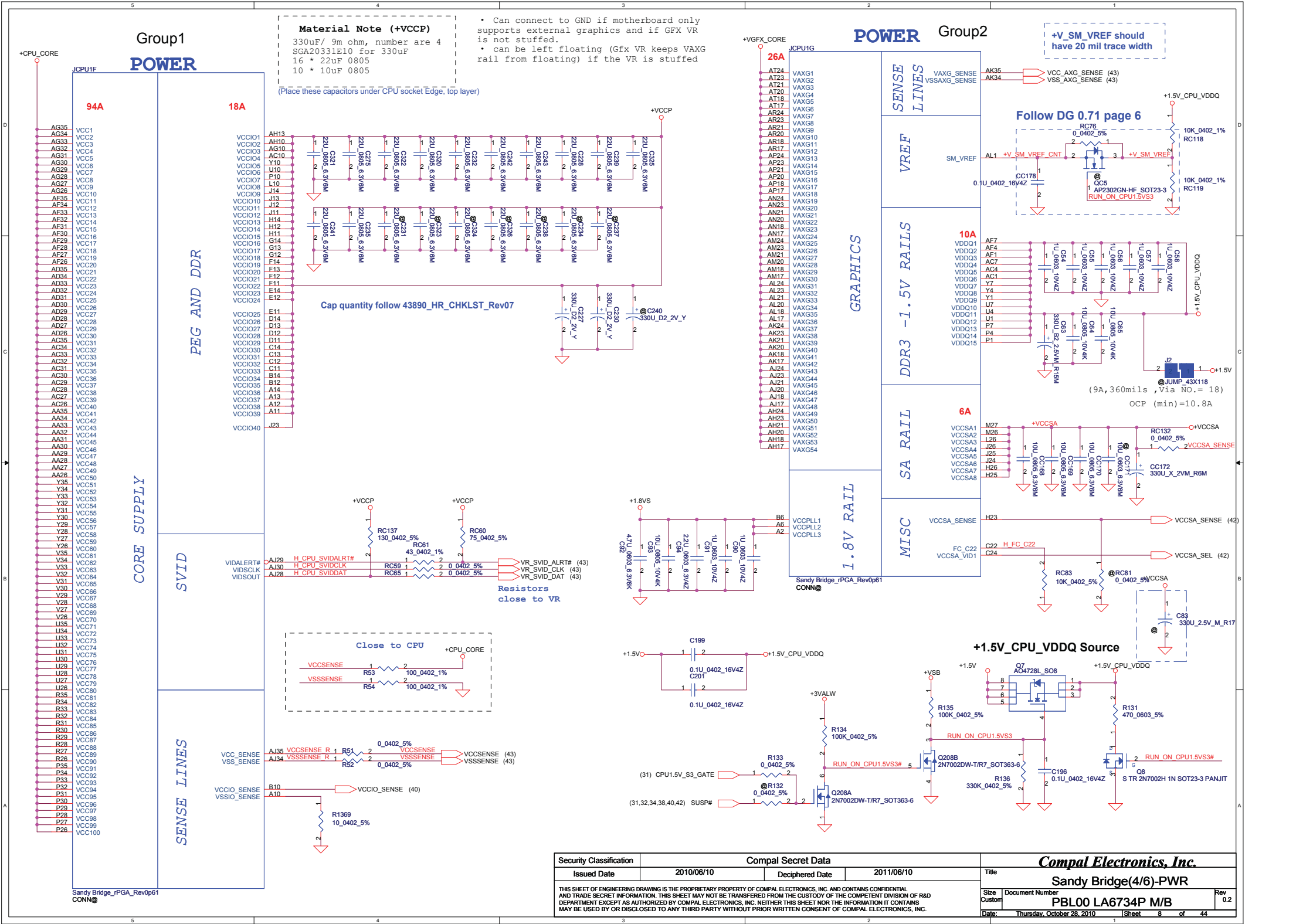
DRAMRST_CNTRL

(31) DRAMRST_CNTRL_EC

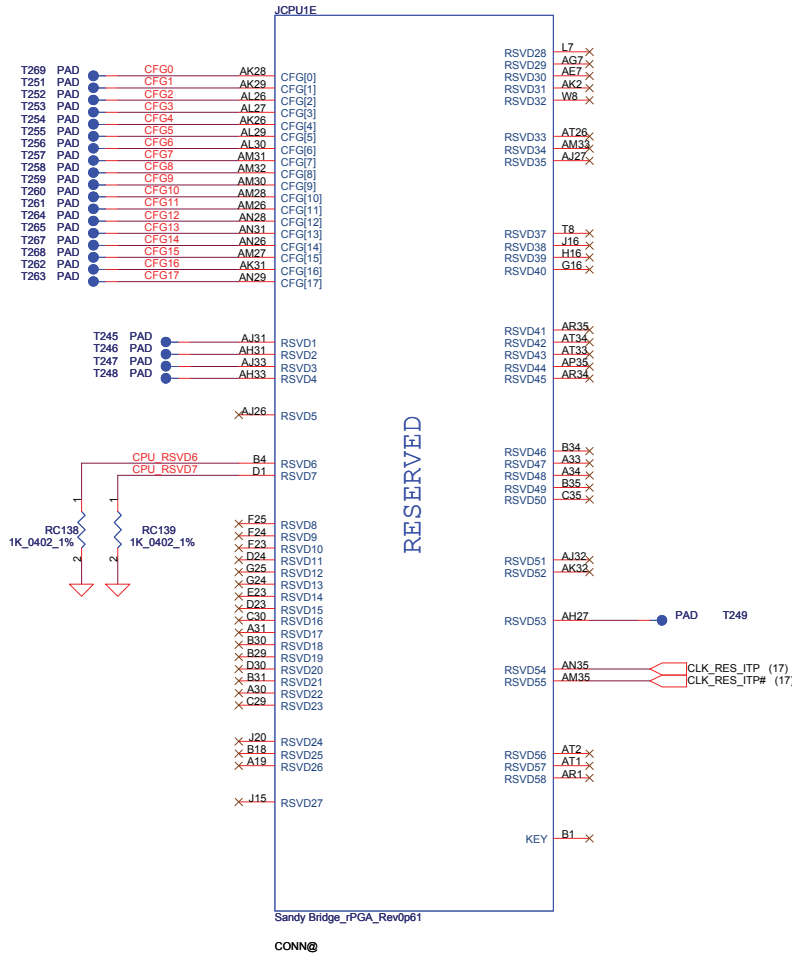
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C86
0.047U_0402_16V4Z

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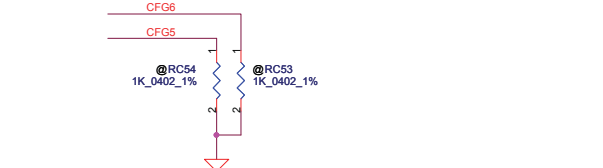
CFG Straps for Processor



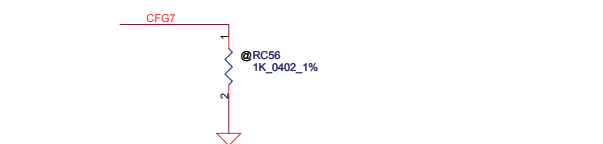
| PEG Static Lane Reversal - CFG2 is for the 16x | |
|--|--|
| CFG2 | 1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed |



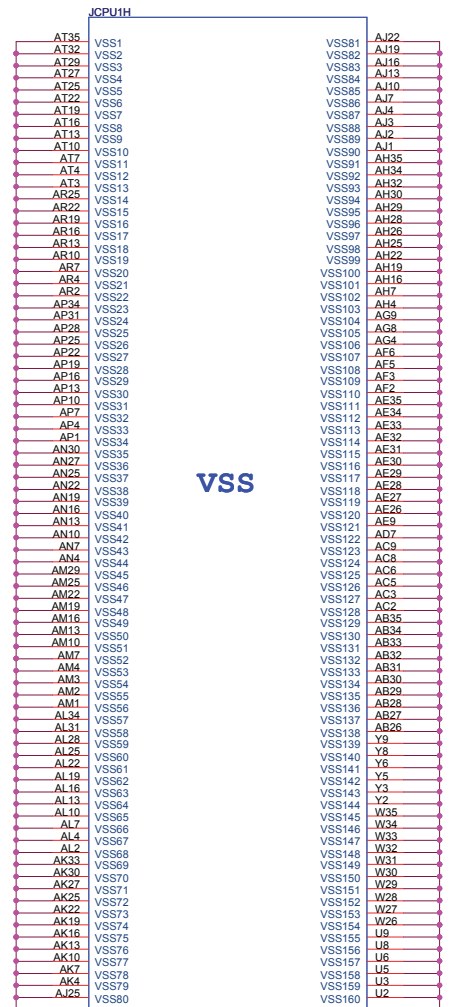
| Display Port Presence Strap | |
|-----------------------------|--|
| CFG4 | * 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port |



| PCIe Port Bifurcation Straps | |
|------------------------------|--|
| CFG[6:5] | * 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled |

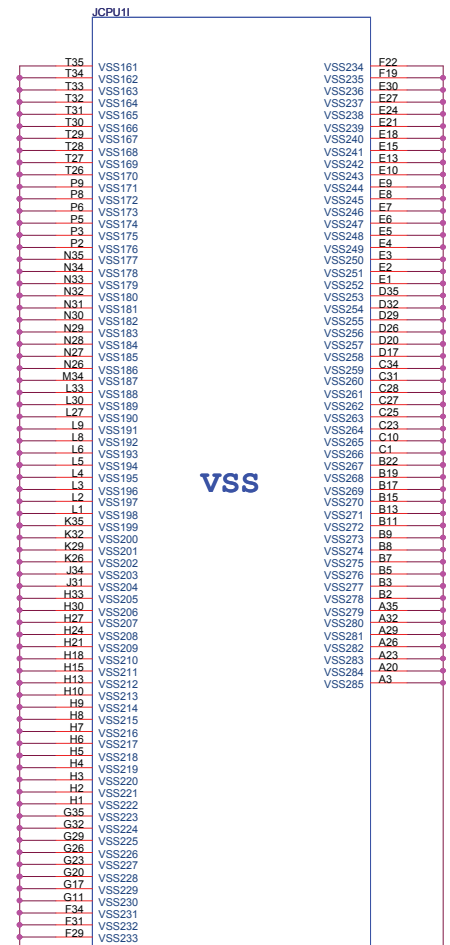


| PEG DEFER TRAINING | |
|--------------------|---|
| CFG7 | * 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training |



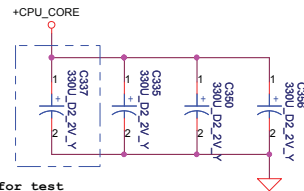
Sandy Bridge_rPGA_Rev0p61

CONN@

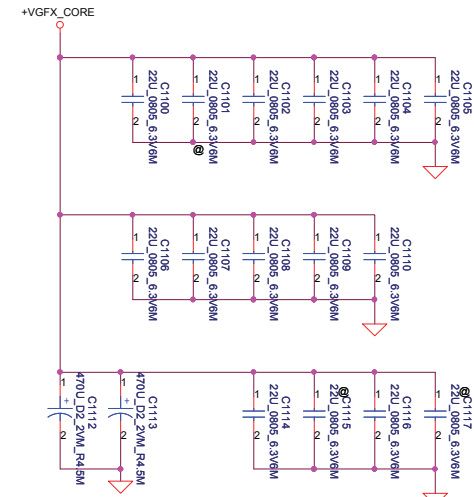


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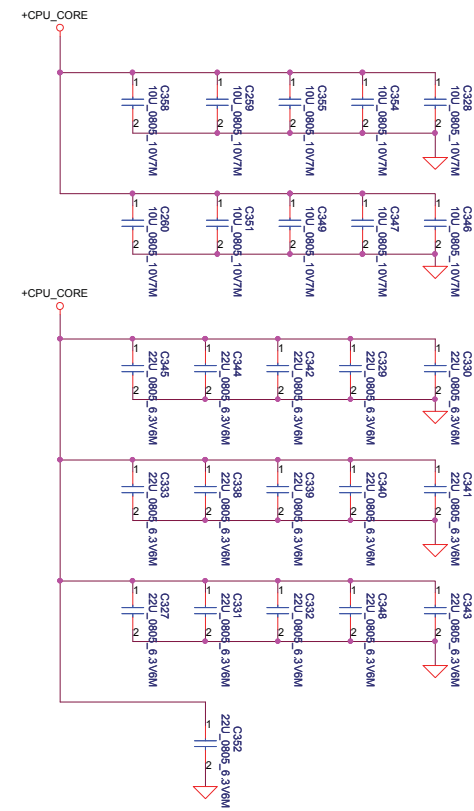
CONN@



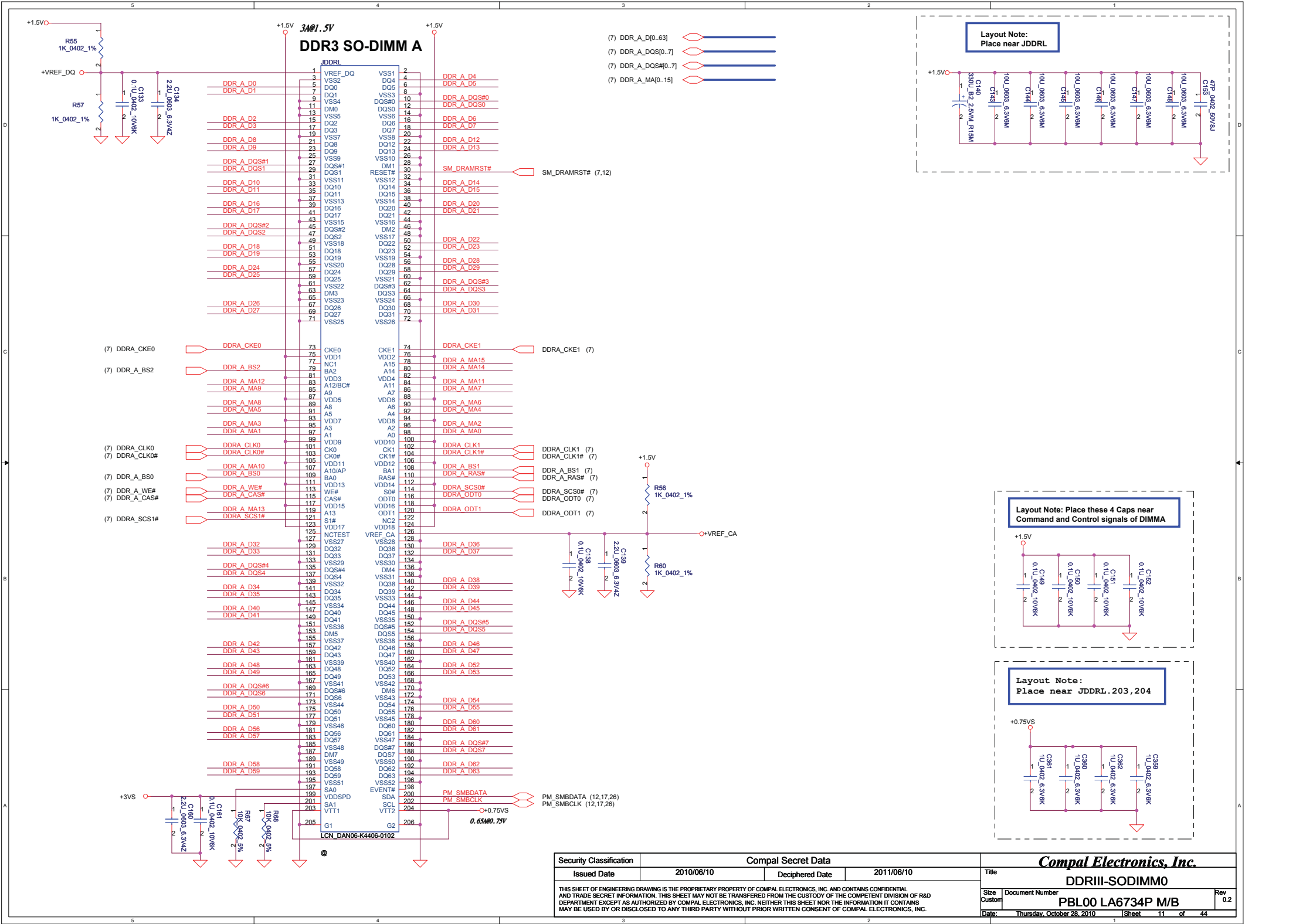
reserve for test
please co-layout with C80



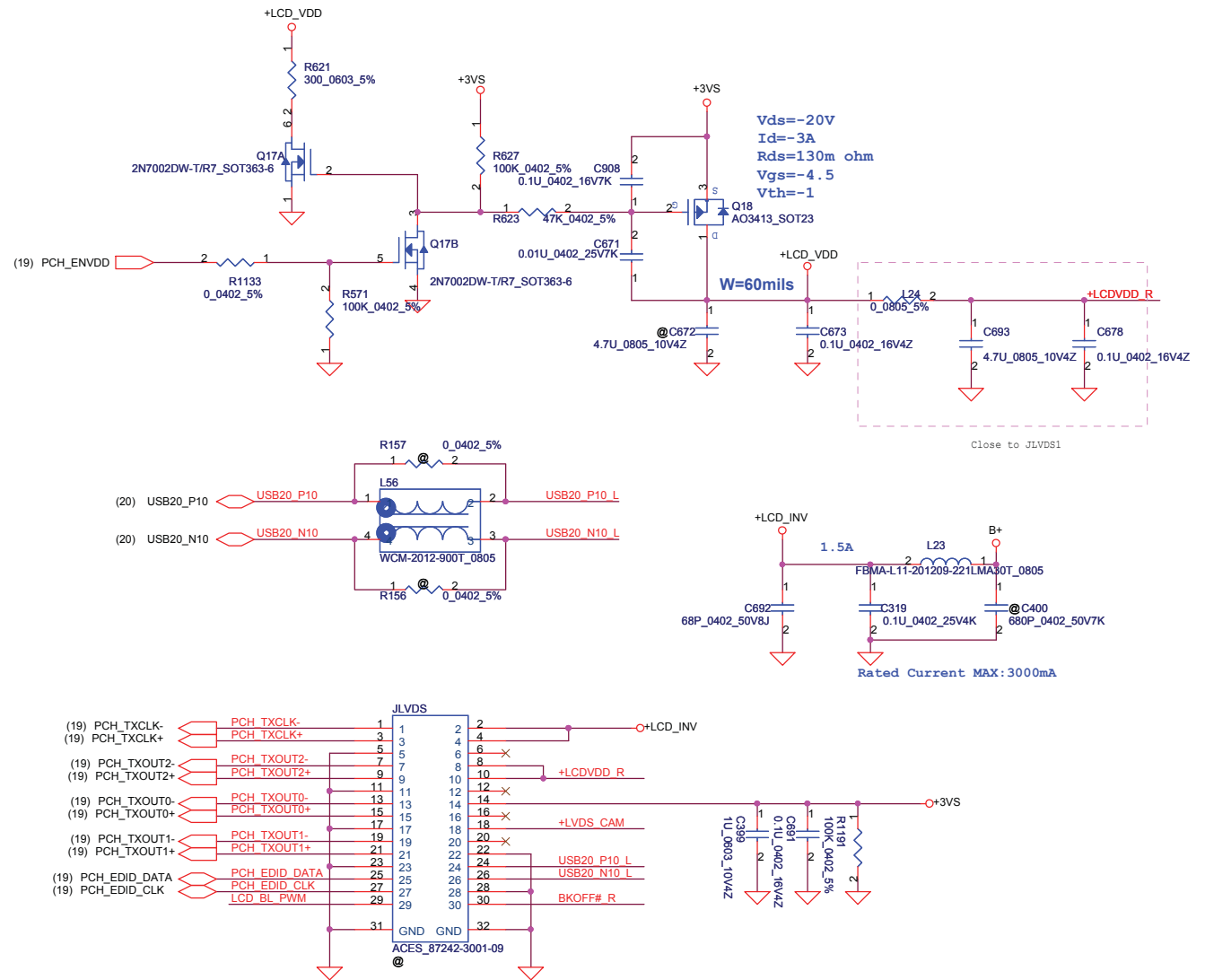
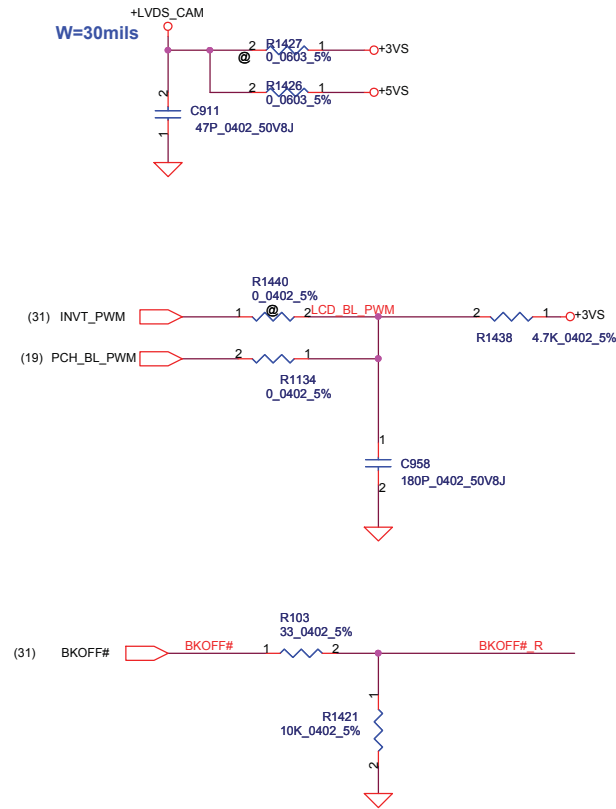
sv type CPU



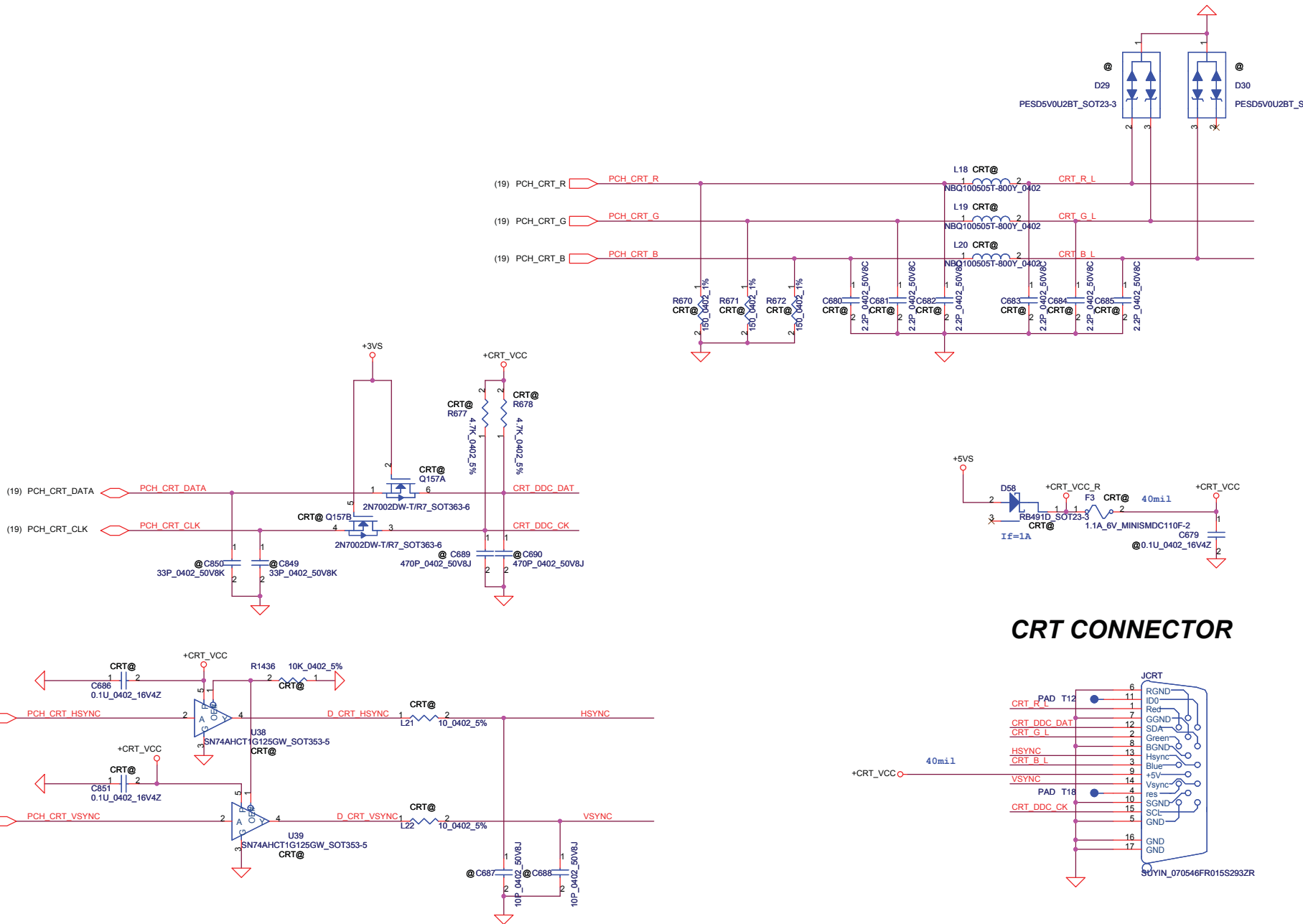
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| | | | | Custom | PBL00 LA6734P M/B | 0.2 |
| | | | | Date | Wednesday, October 27, 2010 | Sheet 10 of 44 |
| | | | | | | |



LCD/PANEL BD. Conn.

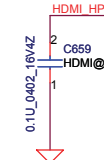
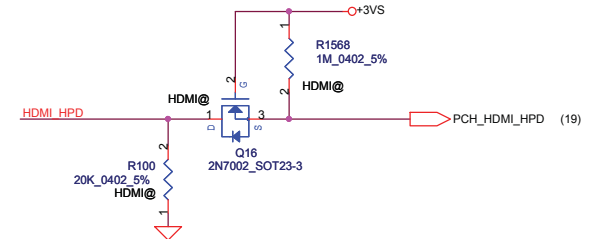
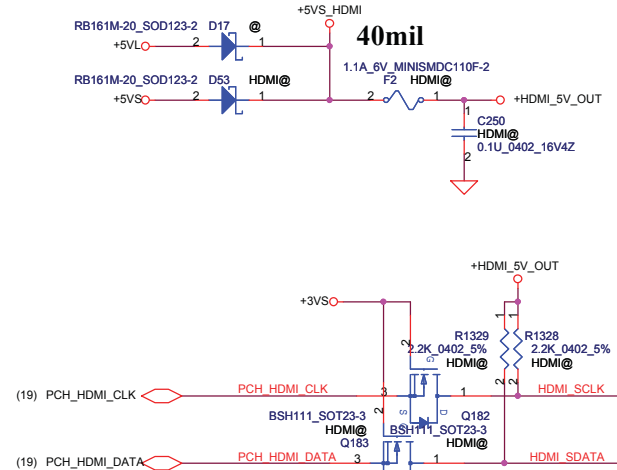
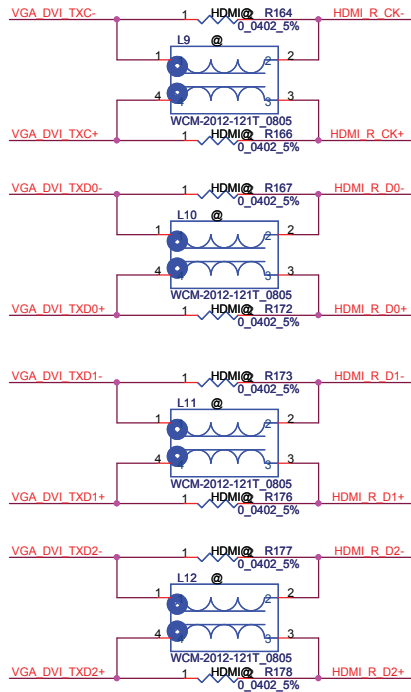


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| | | | | Sheet | 13 of 44 |
| | | | | Rev | 0.2 |

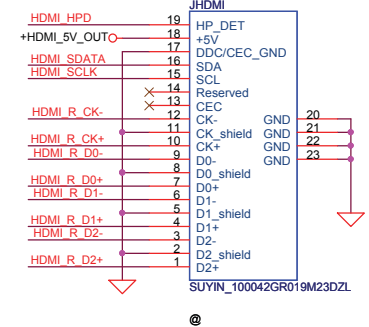
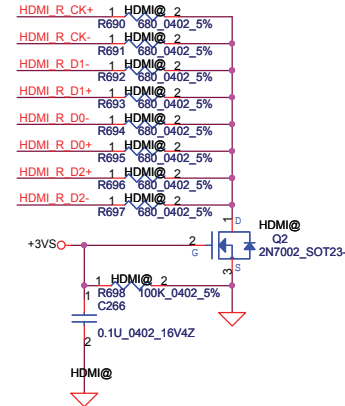


CRT CONNECTOR

| | | | | | |
|---|------------|----------------------------|------------|--------------------------|-----------------|
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| | | | | Size | Document Number |
| | | | | PBL00 LA6734P M/B | |
| Date | | Thursday, October 28, 2010 | | Sheet | 14 of 44 |
| | | | | Rev | 0.2 |

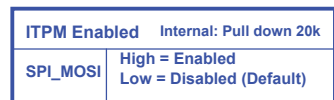
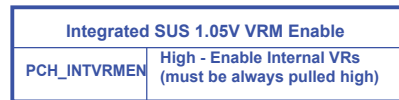
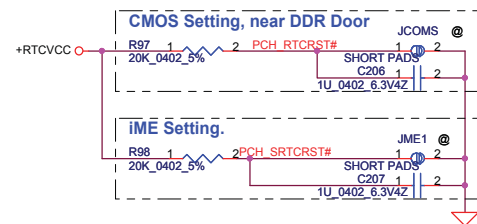


HDMI Connector



| | | | | | | |
|---------------------------|-------|-------|---|---|-----------------|---------------|
| (19) PCIE_MTX_GRX_HDMI_P3 | HDMI@ | CV269 | 1 | 2 | 0.1U_0402_16V7K | VGA DVI TXC+ |
| (19) PCIE_MTX_GRX_HDMI_N3 | HDMI@ | CV270 | 1 | 2 | 0.1U_0402_16V7K | VGA DVI TXC- |
| (19) PCIE_MTX_GRX_HDMI_P2 | HDMI@ | CV271 | 1 | 2 | 0.1U_0402_16V7K | VGA DVI TXD0+ |
| (19) PCIE_MTX_GRX_HDMI_N2 | HDMI@ | CV272 | 1 | 2 | 0.1U_0402_16V7K | VGA DVI TXD0- |
| (19) PCIE_MTX_GRX_HDMI_P1 | HDMI@ | CV273 | 1 | 2 | 0.1U_0402_16V7K | VGA DVI TXD1+ |
| (19) PCIE_MTX_GRX_HDMI_N1 | HDMI@ | CV274 | 1 | 2 | 0.1U_0402_16V7K | VGA DVI TXD1- |
| (19) PCIE_MTX_GRX_HDMI_P0 | HDMI@ | CV275 | 1 | 2 | 0.1U_0402_16V7K | VGA DVI TXD2+ |
| (19) PCIE_MTX_GRX_HDMI_N0 | HDMI@ | CV276 | 1 | 2 | 0.1U_0402_16V7K | VGA DVI TXD2- |

| | | | | | |
|---|----------------------------|--------------------|------------|--------------------------|-----|
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| Issued Date | 2010/06/10 | Deciphered Date | 2011/06/10 | Title | |
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| Size | Document Number | PBL00 LA6734P M/B | | Rev | 0.2 |
| Date: | Thursday, October 28, 2010 | Sheet | 15 | of | 44 |

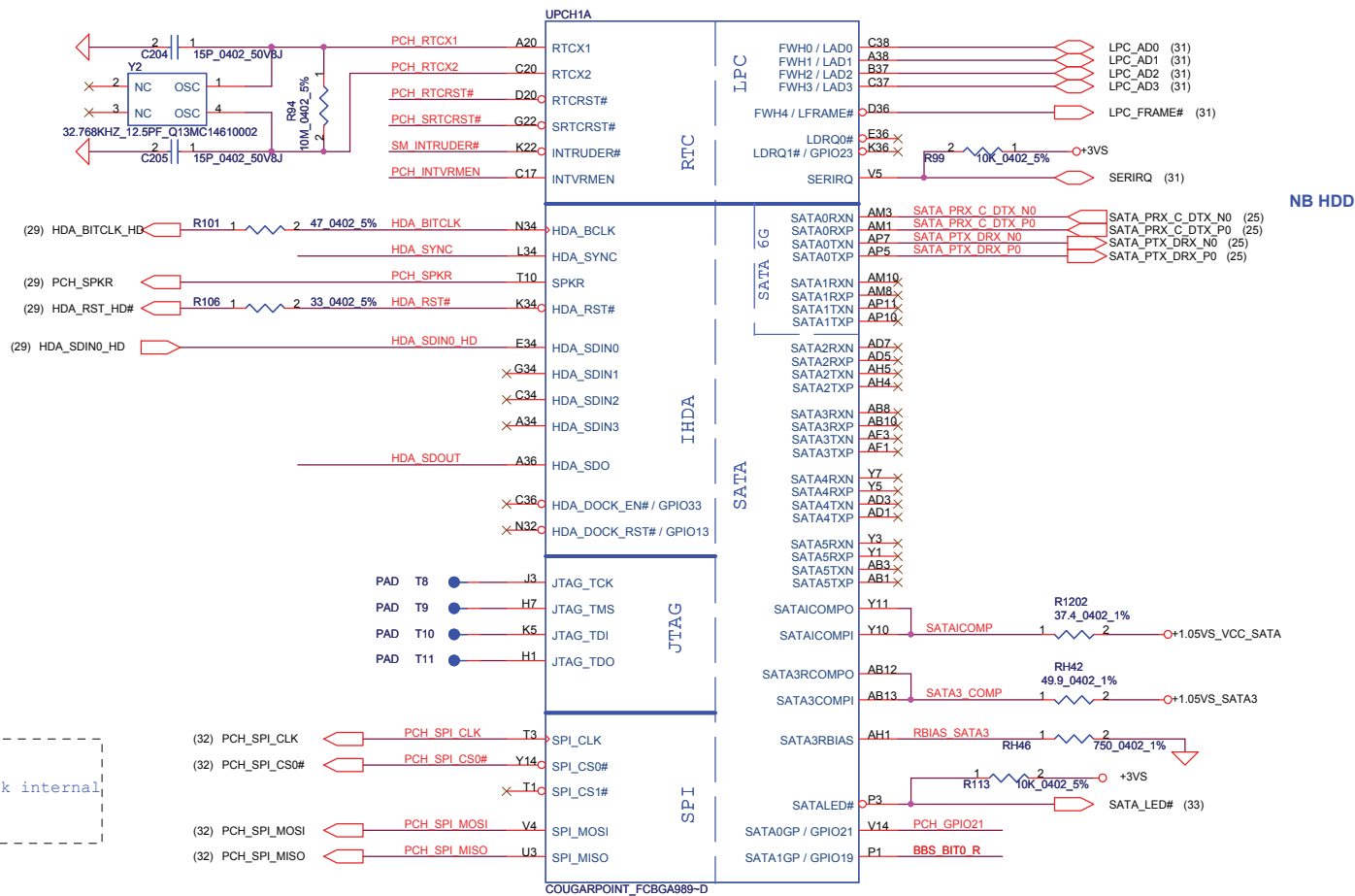
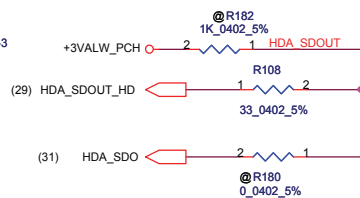
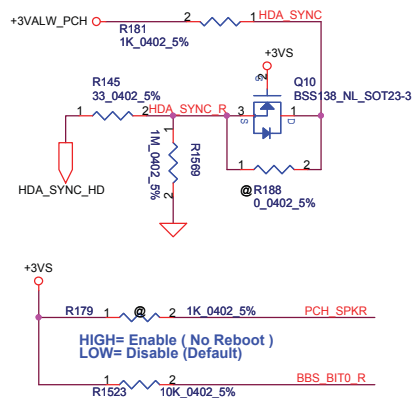


HDA_SYNC

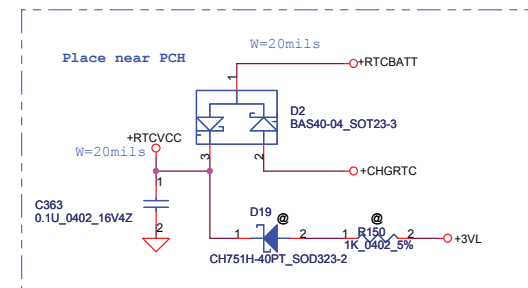
This signal has a weak internal pull down.
H=>On Die PLL is supplied by 1.5V
*L=>On Die PLL is supplied by 1.8V

HDA_SDO

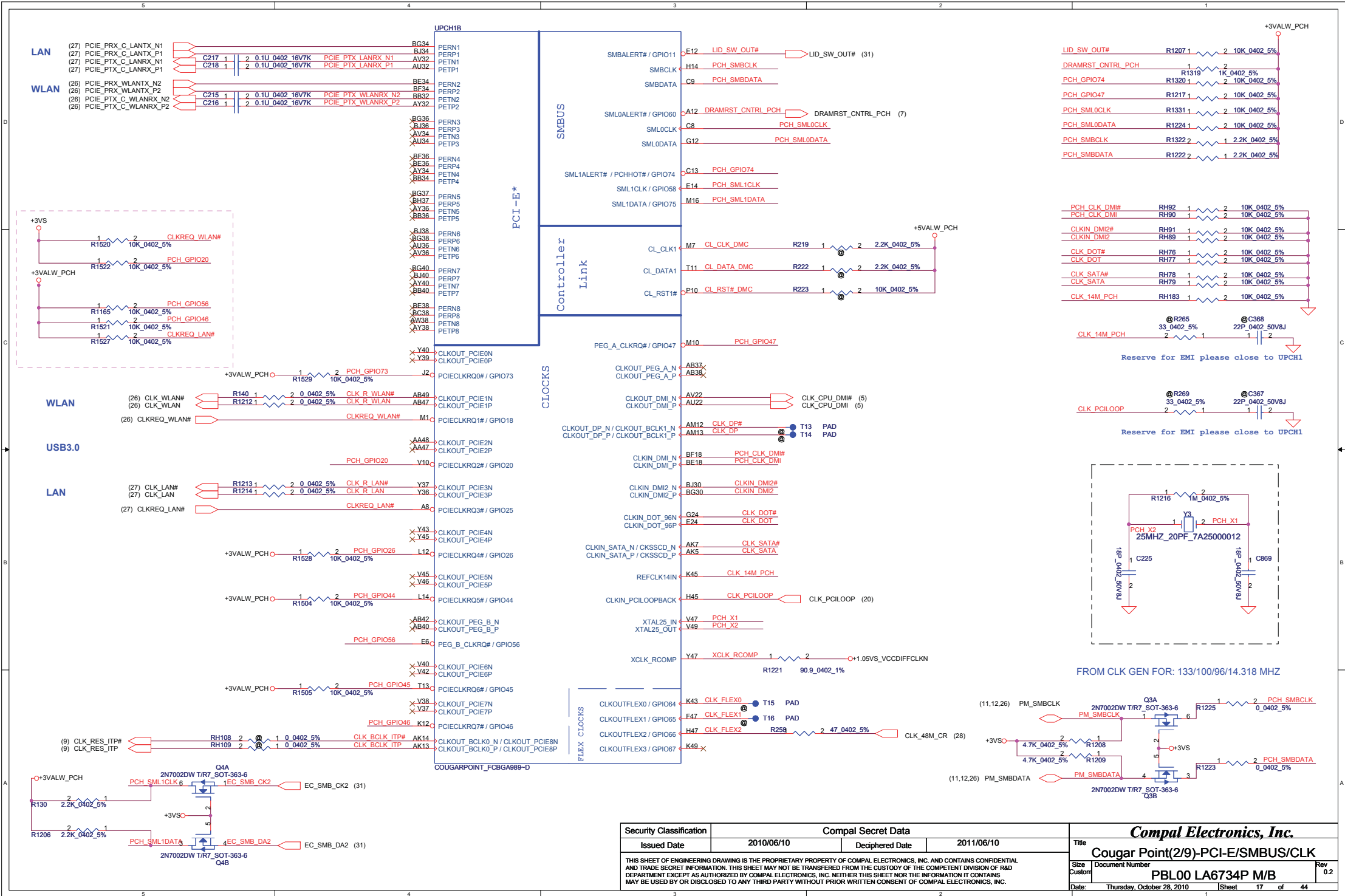
This signal has a weak internal pull down.
This signal can't PU

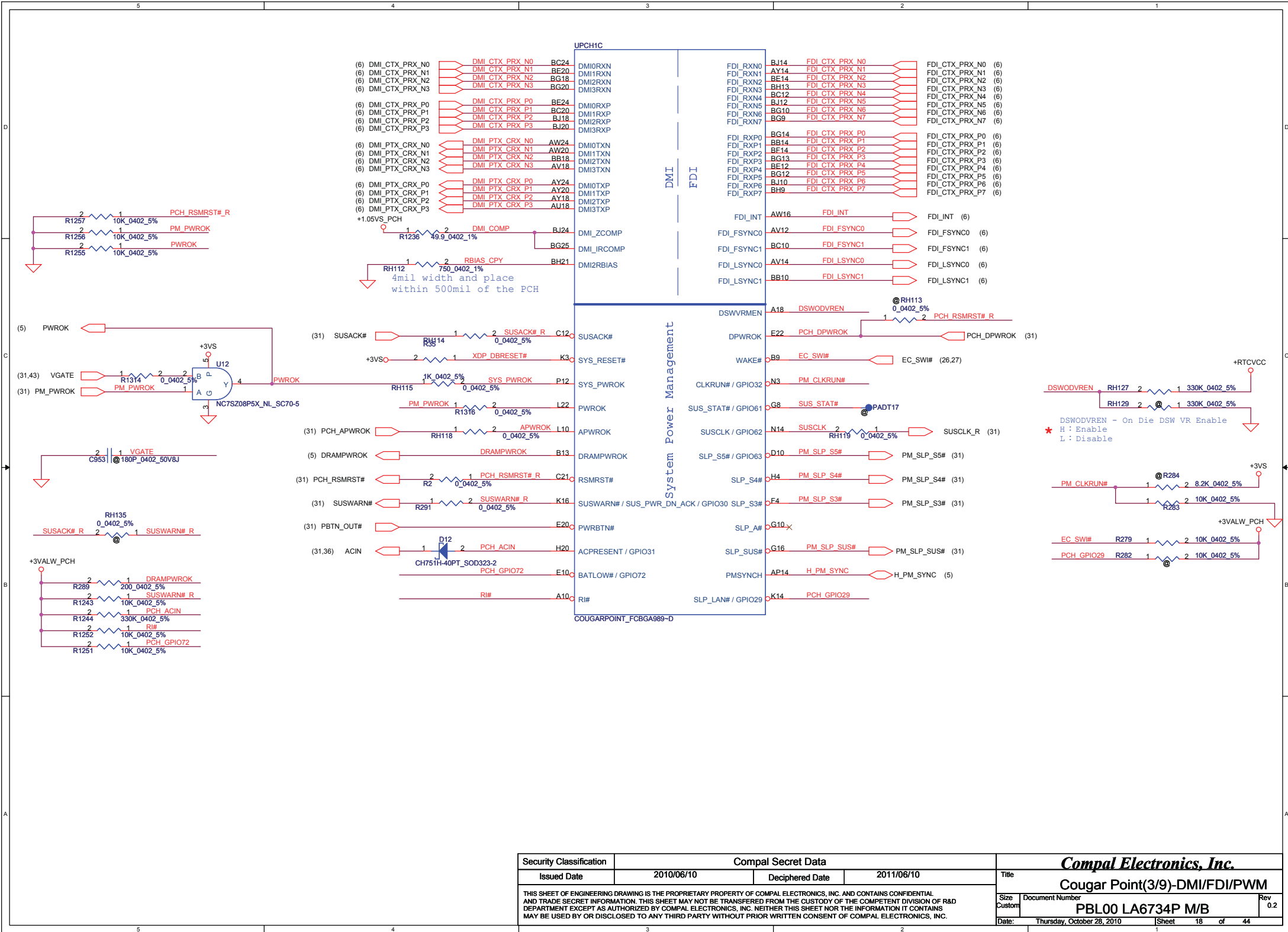


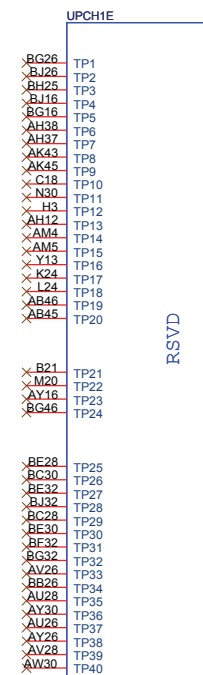
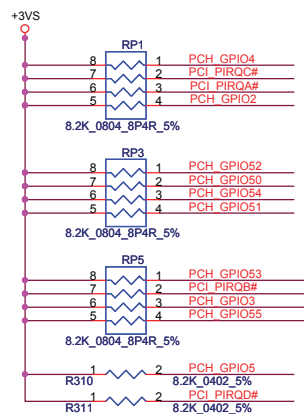
| Project ID | GPIO21 |
|------------|--------|
| ★ 13" | 0 |
| 14" | 1 |

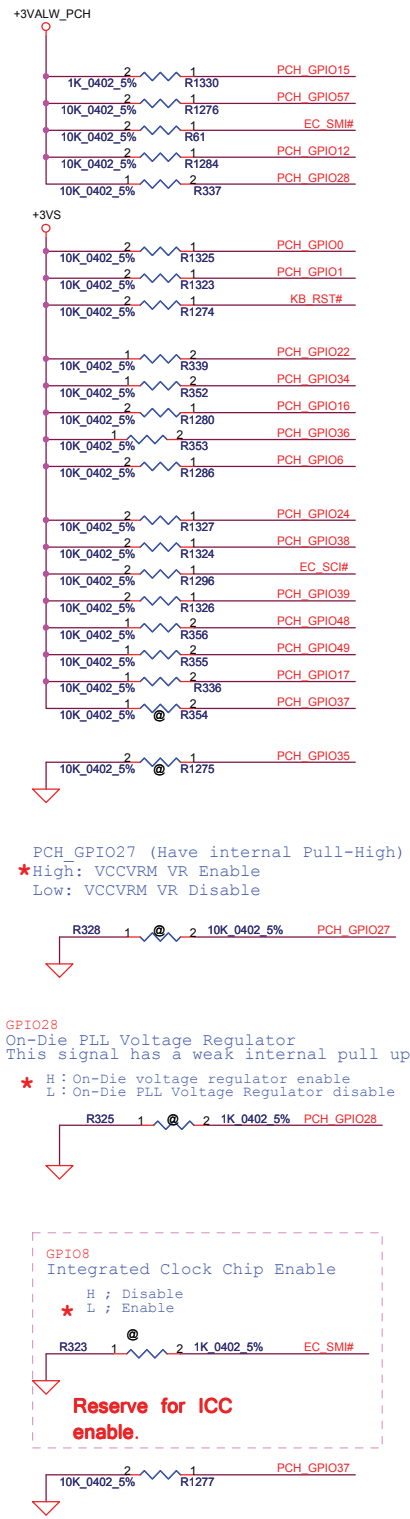


| | | | | | |
|---|------------|--------------------|------------|--------------------------|------------------------------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2010/06/10 | Deciphered Date | 2011/06/10 | Title | Cougar Point(1/9)-HDA/SATA/RTC/SPI |
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| | | | | Date: | Thursday, October 28, 2010 |
| | | | | Sheet | 16 of 44 |

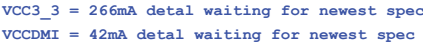


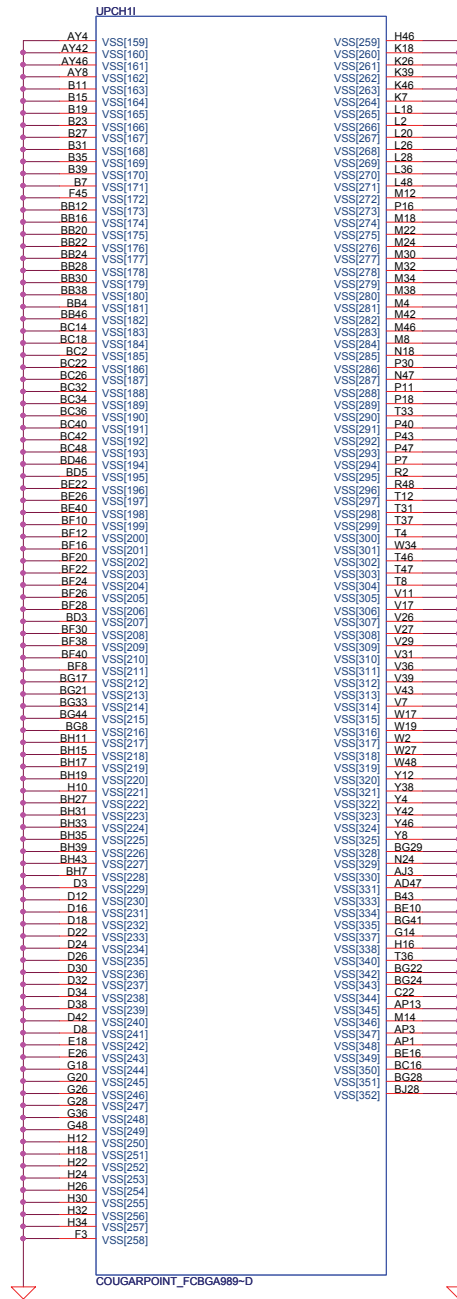
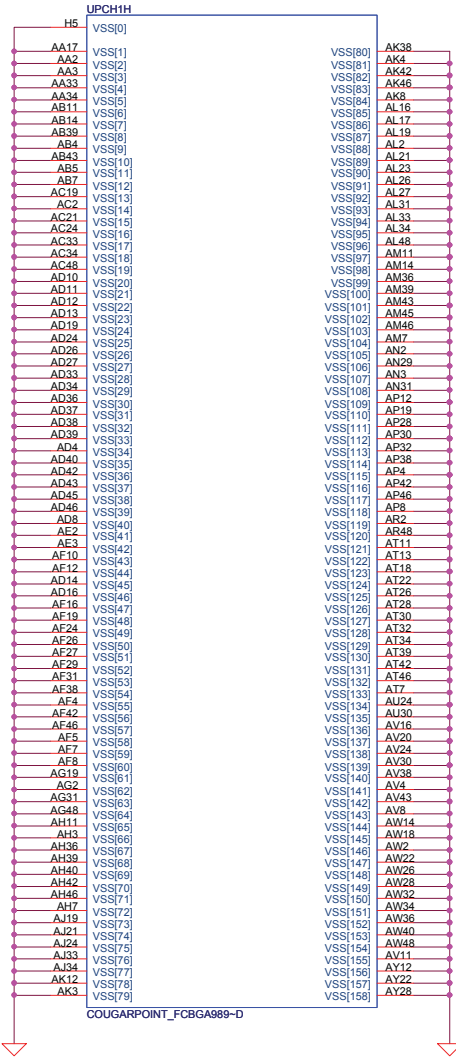






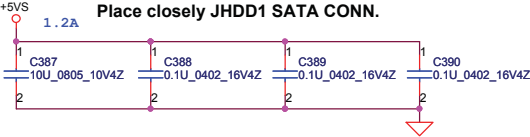
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|---|------------|--------------------|------------|--------------------------|---------------------------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2010/06/10 | Deciphered Date | 2011/06/10 | Title | Cougar Point(6/9)-CPU/GPIO/MISC |
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| | | | | Date: | Thursday, October 28, 2010 |
| | | | | Sheet | 21 of 44 |
| | | | | Rev | 0.2 |



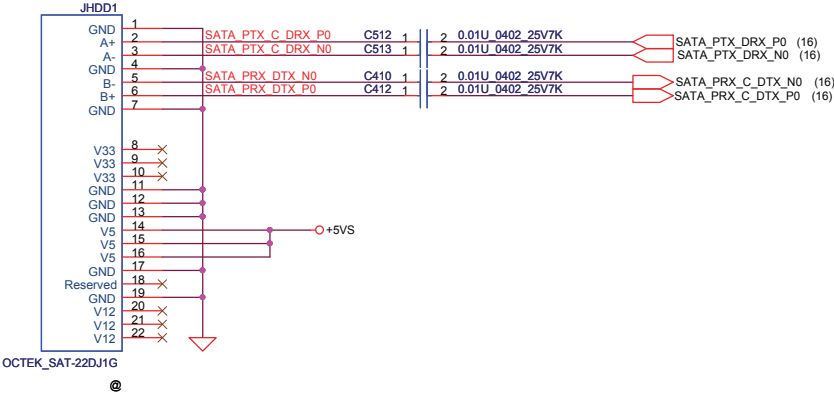


| | | | | | | | |
|---|--|-----------------------------|--|---------------------------------|--|------------|--|
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| | | | | Cougar Point(9/9)-GND | | | |
| Size | | Document Number | | PBL00 LA6734P M/B | | Rev 0.2 | |
| Date: | | Tuesday, September 07, 2010 | | Sheet 24 of 44 | | | |

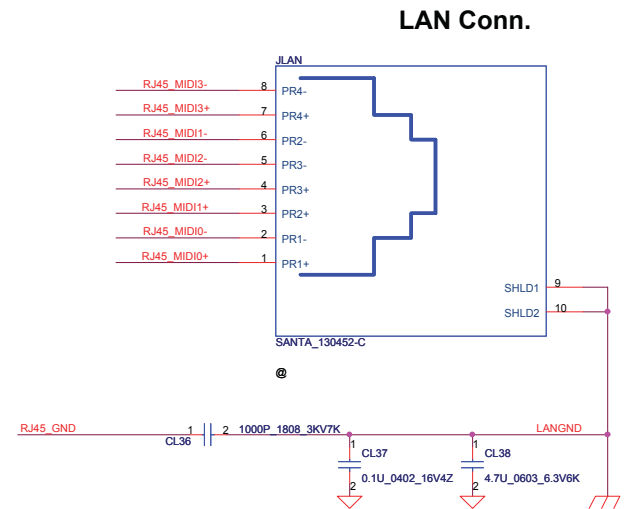
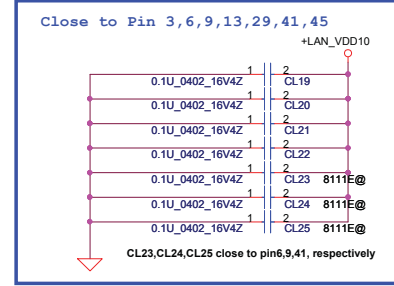
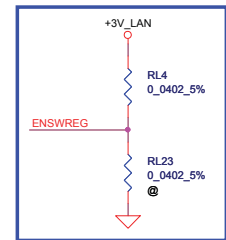
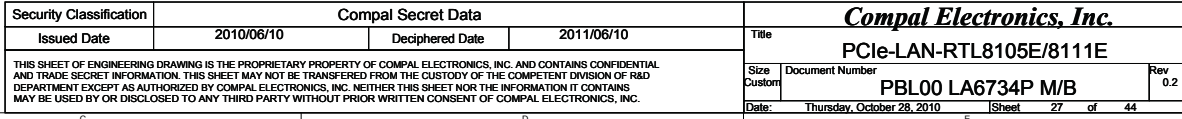
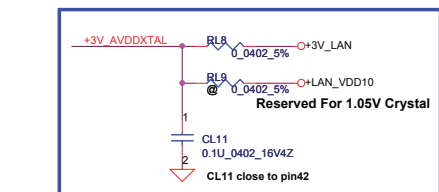
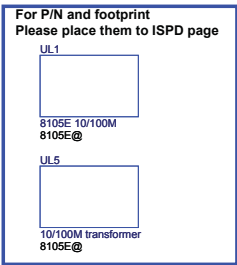
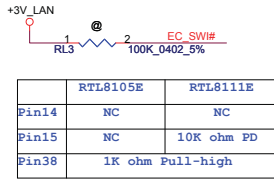
SATA HDD1 Conn.

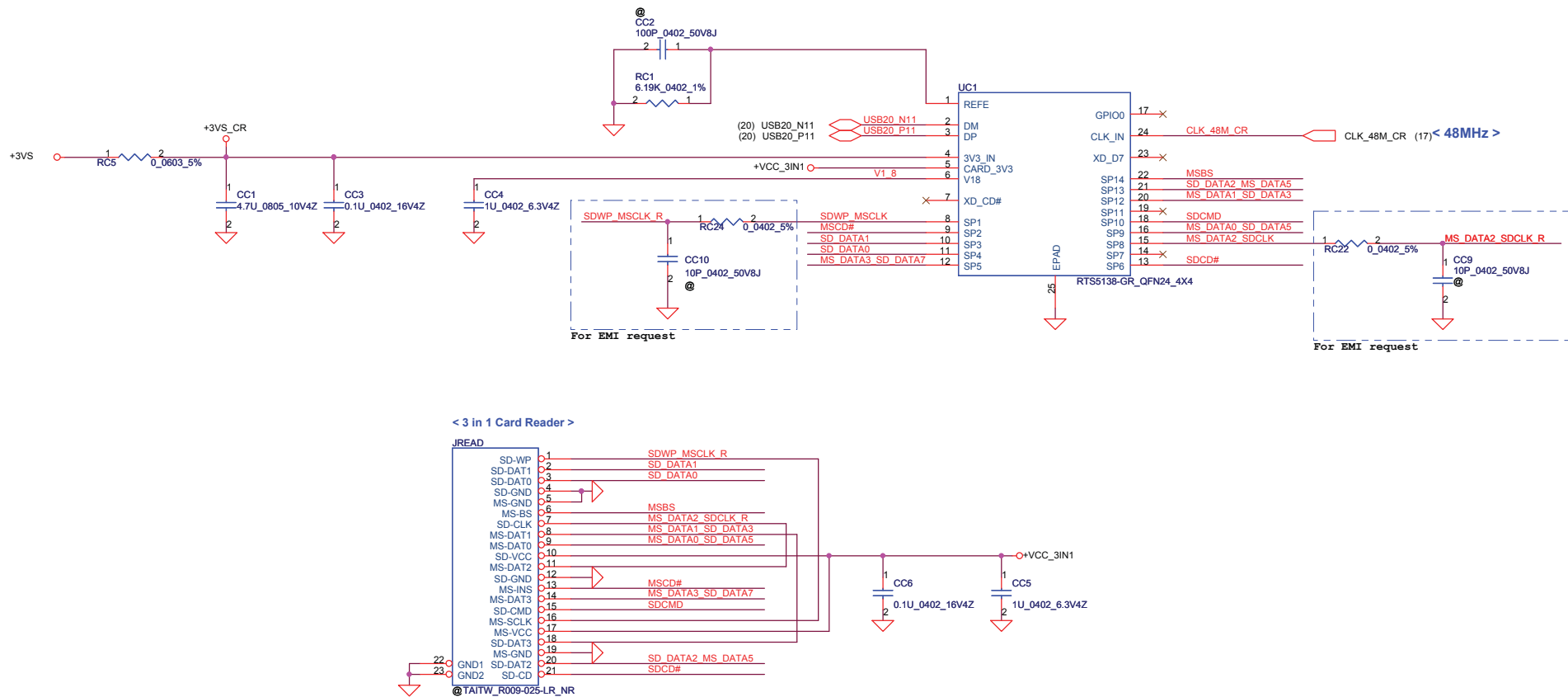


13.3" HDD



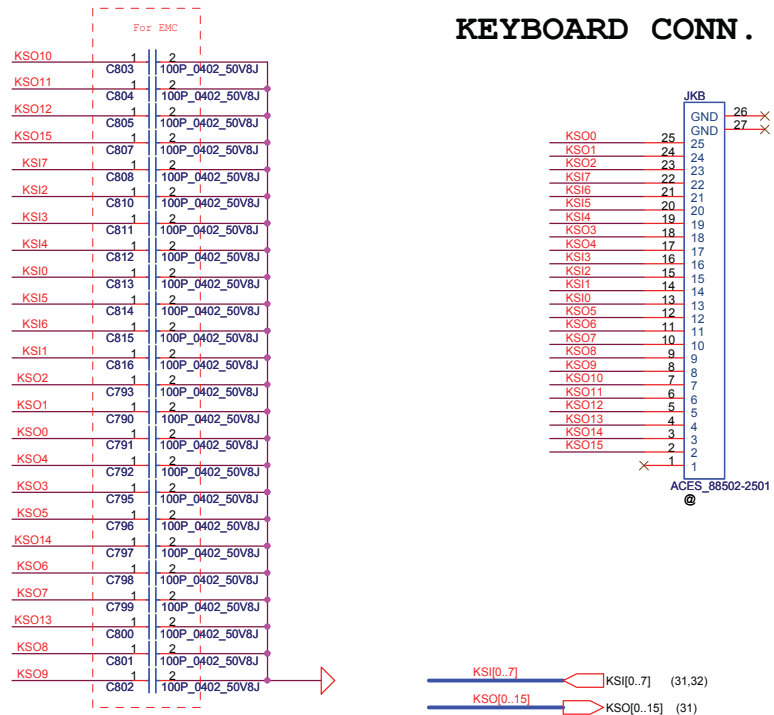
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|---|----------------------------|--------------------|------------|--------------------------|----|
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| | PBL00 LA6734P M/B | | | 0.2 | |
| Date: | Thursday, October 28, 2010 | Sheet | 25 | of | 44 |



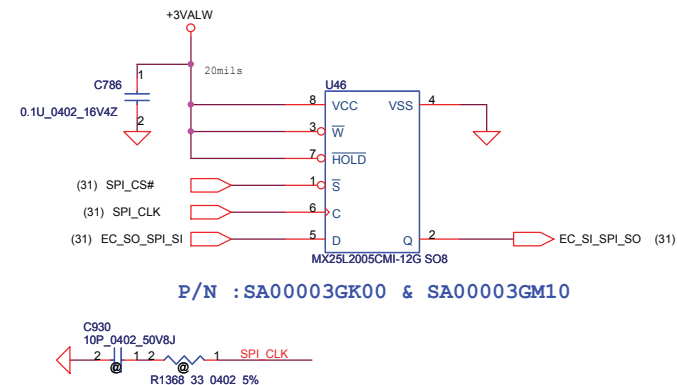


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|---|--|--------------------|--|---------------------------------|--|-------------------|--|-------------------------|--|
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| | | | | | | | | USB-Card Reader-RTS5138 | |
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| | | | | | | | | | |
| | | | | | | | | | |
| Date: | | | | Thursday, October 28, 2010 | | Sheet 28 of 44 | | | |

KEYBOARD CONN.



SPI Flash (1MByte*1)



ISPD

PCB

ZZZ

PCB LA-6734P REV01

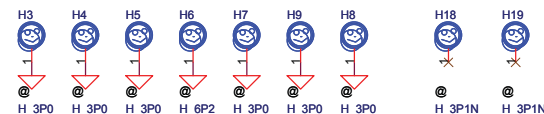
DC-IN

PJPDC1

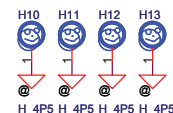
PJPDC1

45②

Screw Hole



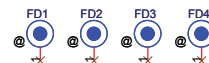
CPU



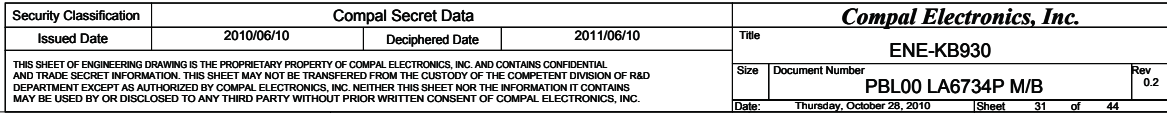
JWLAN



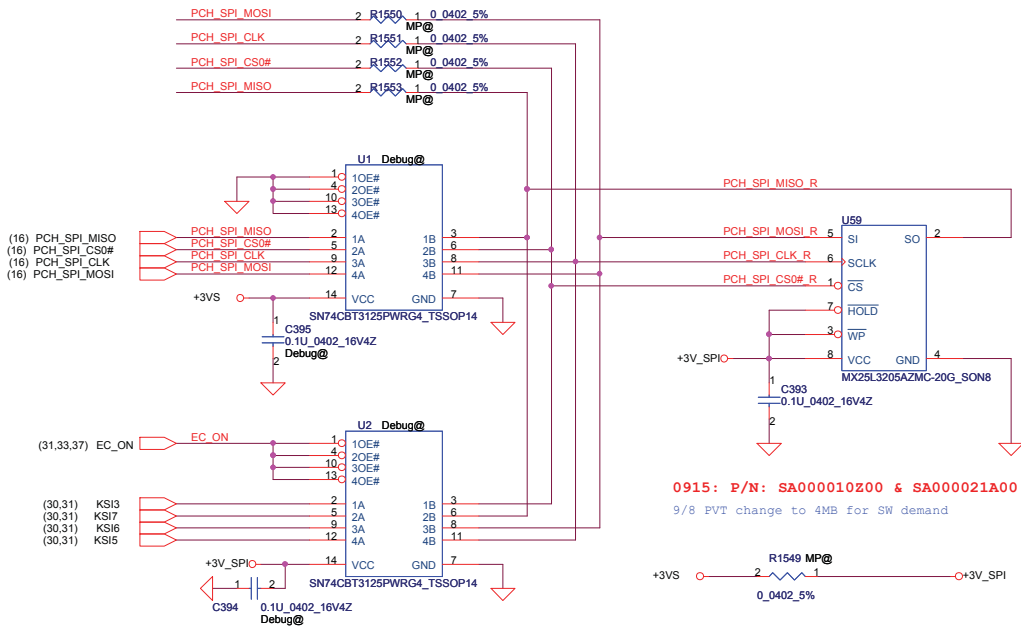
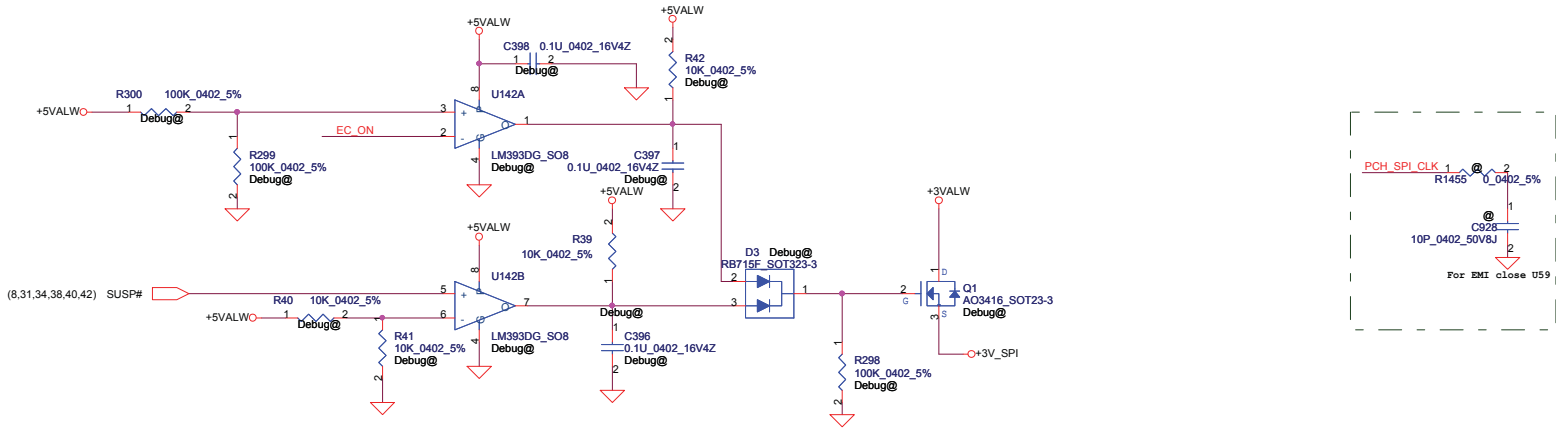
PCB Fedcal Mark PAD



| | | | | | |
|---|----------------------------|-------------------|------------|--------------------------|---------|
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| Size | Document Number | PBL00 LA6734P M/B | | | Rev 0.2 |
| Date: | Thursday, October 28, 2010 | Sheet | 30 | of | 44 |



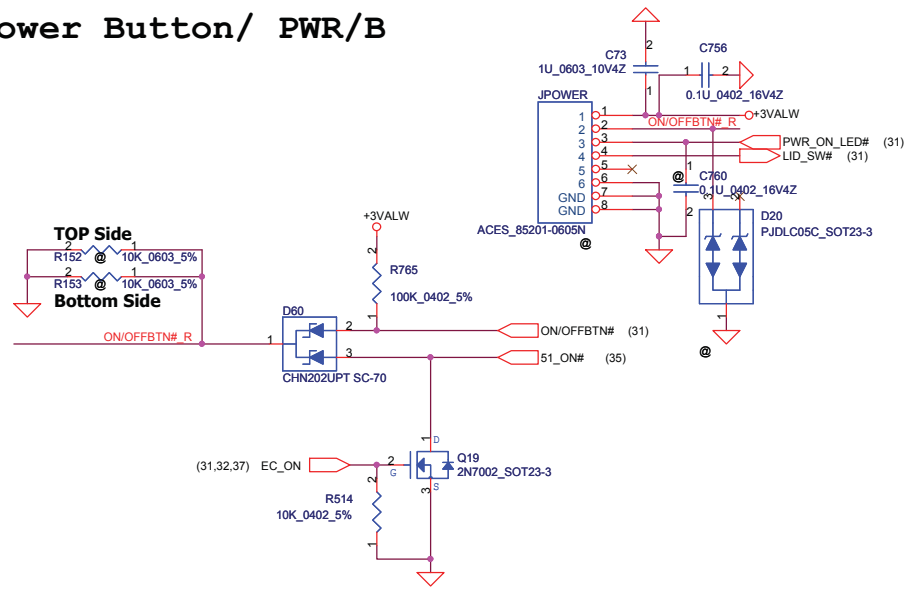
SPI ROM For Basic ME ROM size
(w/o Braidwood & system BIOS):
4MByte



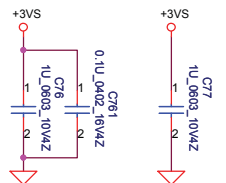
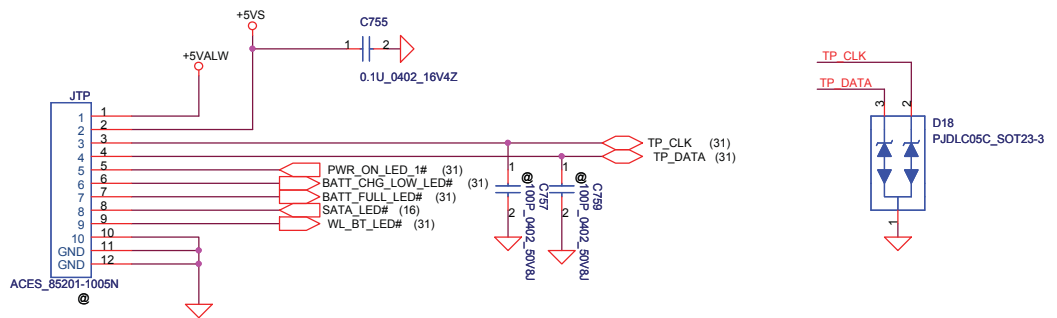
0915: P/N: SA000010X00 & SA000021A00
9/8 PVT change to 4MB for SW demand

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|---|------------|--------------------|------------|-------------------|----------------------------|
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| | | | | PBL00 LA6734P M/B | |
| | | | | Date | Thursday, October 28, 2010 |
| | | | | Sheet | 32 of 44 |

Power Button/ PWR/B



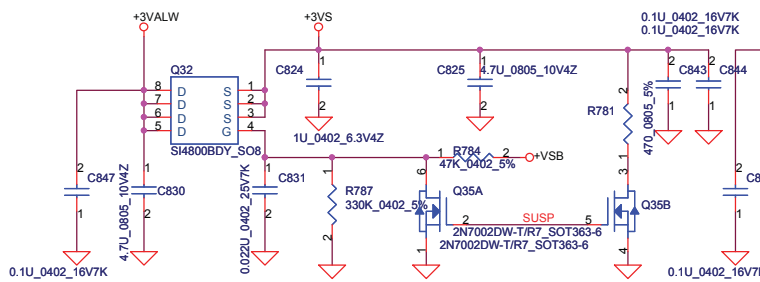
Touch/B Connector



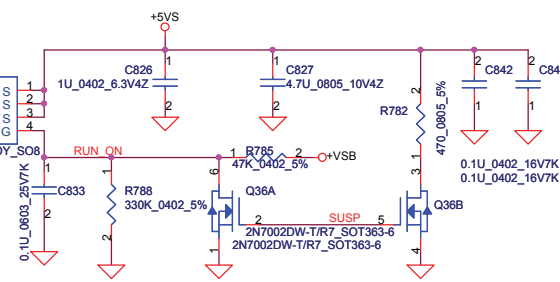
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| Security Classification | | Compal Secret Data | | | | Compal Electronics, Inc. | | | |
| Issued Date | | 2010/06/10 | | Deciphered Date | | 2011/06/10 | | Title | |
| | | | | | | | | PWR/TP/LED | |
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| Size | | Document Number | | | | PBL00 LA6734P M/B | | Rev 0.2 | |
| Date: | | Thursday, October 28, 2010 | | Sheet | | 33 | | of 44 | |

+3VALW TO +3VS

Vgs=-0V, Id=9A, Rds=18.5mohm

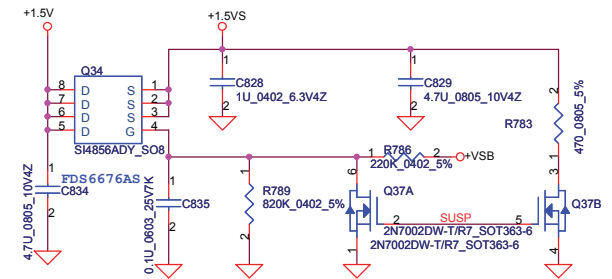


+5VALW TO +5VS



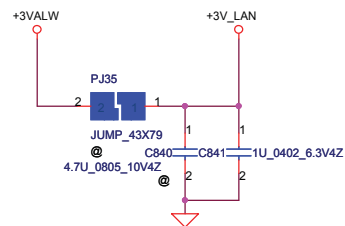
+1.5V to +1.5VS

Vgs=10V, Id=14.5A, Rds=6mohm



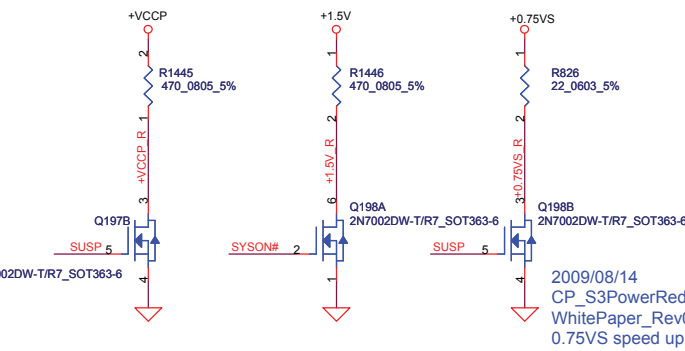
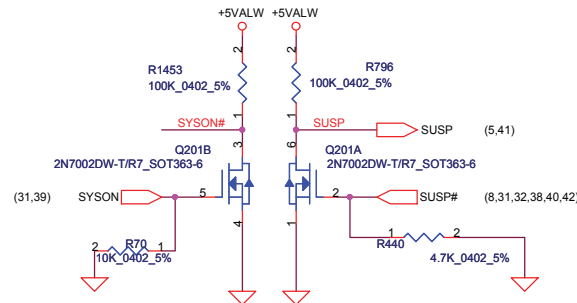
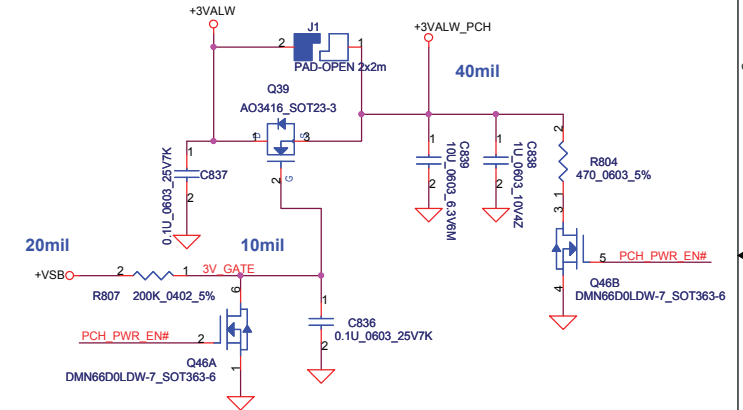
+3VALW TO +3V_LAN

Vgs=-4.5V, Id=3A, Rds<97mohm

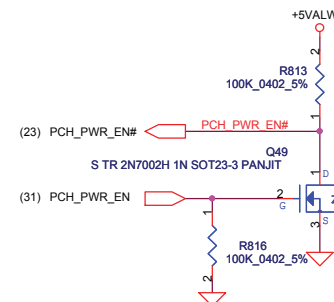


+3VALW TO +3VALW(PCH AUX Power)

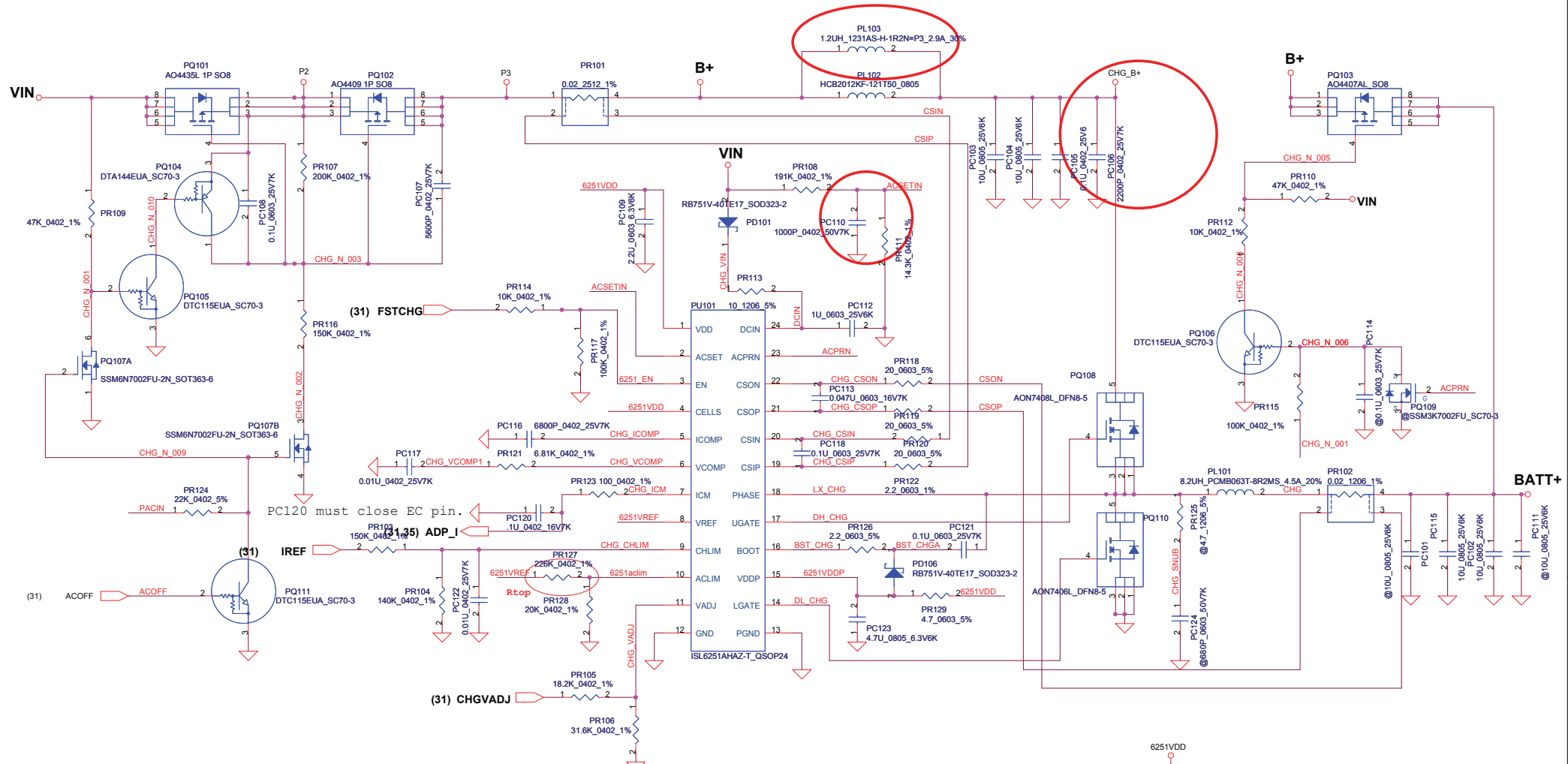
Short J1 for PCH VCCSUS3.3



2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge



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| Size | Document Number | PBL00 LA6734P M/B | | Rev | |
| Date: | | Thursday, October 28, 2010 | | Sheet 34 of 44 | |

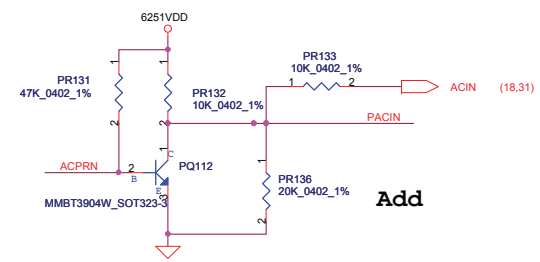


$CP = 85\% \cdot I_{ada}$
 $I_{ada} = 0 \sim 4.737A (90W); CP = 4.03A$; where $R_{acdet} = 0.020\Omega$; where $R_{top} = 12.4K$
 90W for Dis: $R_{top} = SD00000AJ80$
 $I_{ada} = 0 \sim 3.421A (65W); CP = 2.91A$; where $R_{acdet} = 0.020\Omega$; where $R_{top} = 226K$
 65W for UMA: $R_{top} = SD034226380$
 Astro2010_01_15 need confirm P/N

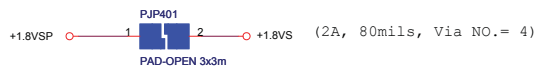
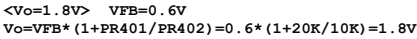
CP mode
 $V_{acim} = V_{REF} \cdot (R_{bot} // R_{internal} / (R_{top} // R_{internal} + R_{bot} // R_{internal}))$
 when 90W $V_{acim} = 2.39 \cdot (20K // 152K / (20K // 152K + 12.4K // 152K)) = 1.44966V$
 when 65W $V_{acim} = 2.39 \cdot (20K // 152K / (20K // 152K + 226K // 152K)) = 0.38914V$
 $I_{input} = (1 / R_{acdet}) \cdot ((0.05 \cdot V_{acim} / V_{REF} + 0.05))$
 when 90W, $I_{input} = (1 / 0.02) \cdot ((0.05 \cdot 1.44966 / 2.39 + 0.05)) = 4.02A$
 when 65W, $I_{input} = (1 / 0.02) \cdot ((0.05 \cdot 0.38914 / 2.39 + 0.05)) = 2.92A$

$CC = 0.25A \sim 3A$
 $I_{REF} = 1.016 \cdot I_{charge}$
 $I_{REF} = 0.254V \sim 3.048V$
 V_{CHLIM} need over 95mV

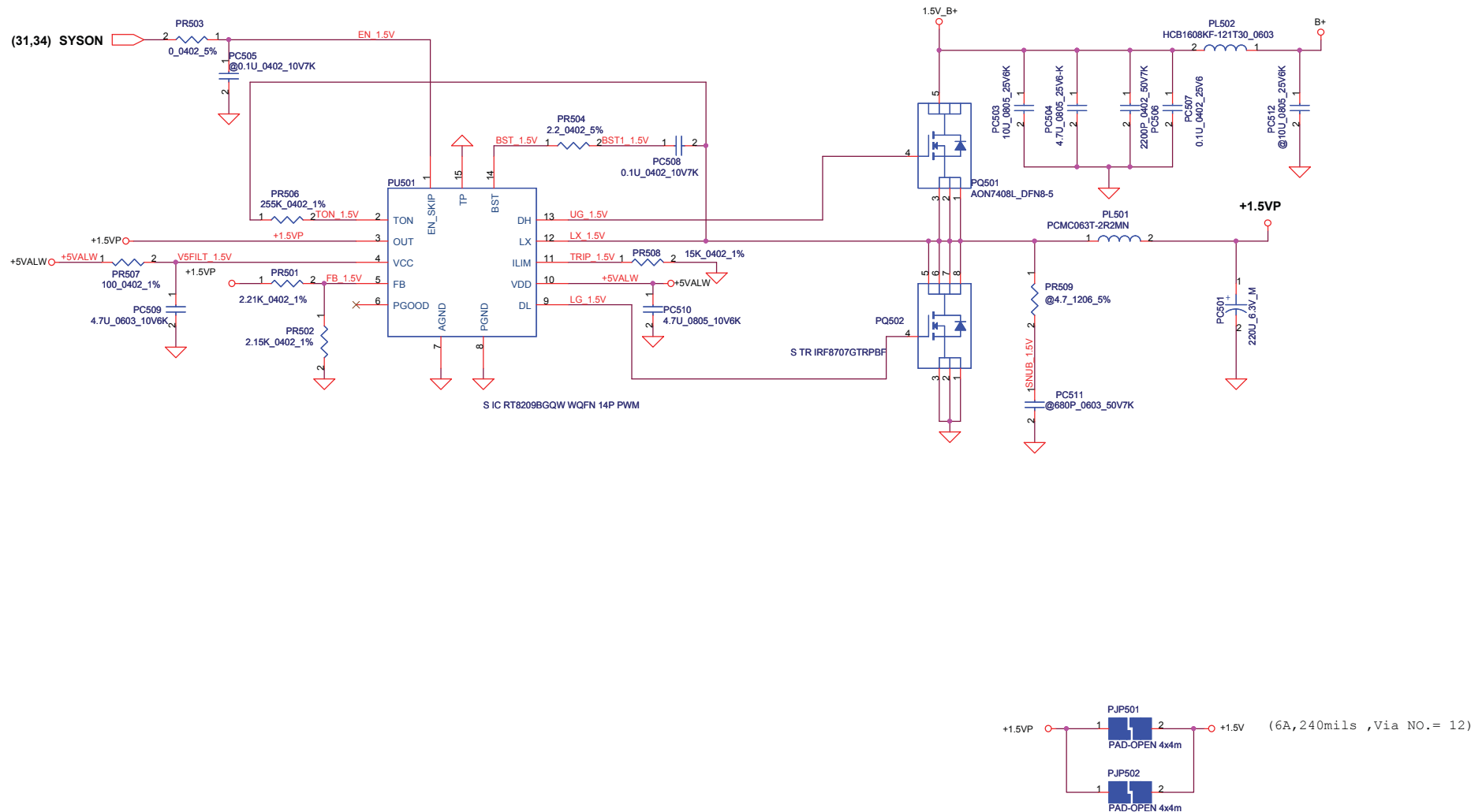
| CHGVADJ=(Vcell-4)/0.10627 | |
|---------------------------|---------|
| Vcell | CHGVADJ |
| 4V | 0V |
| 4.2V | 1.882V |

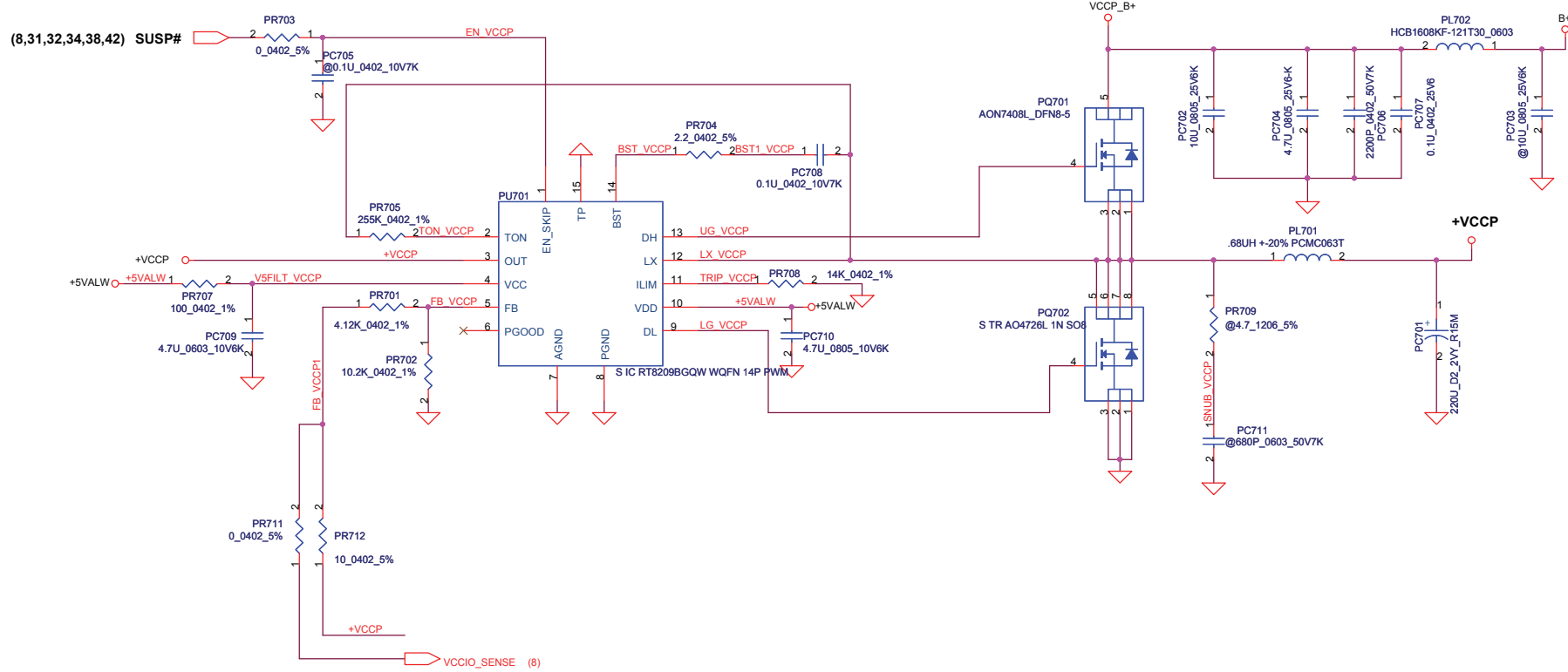


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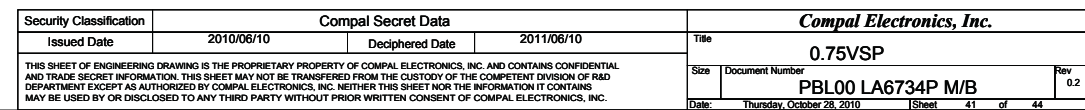
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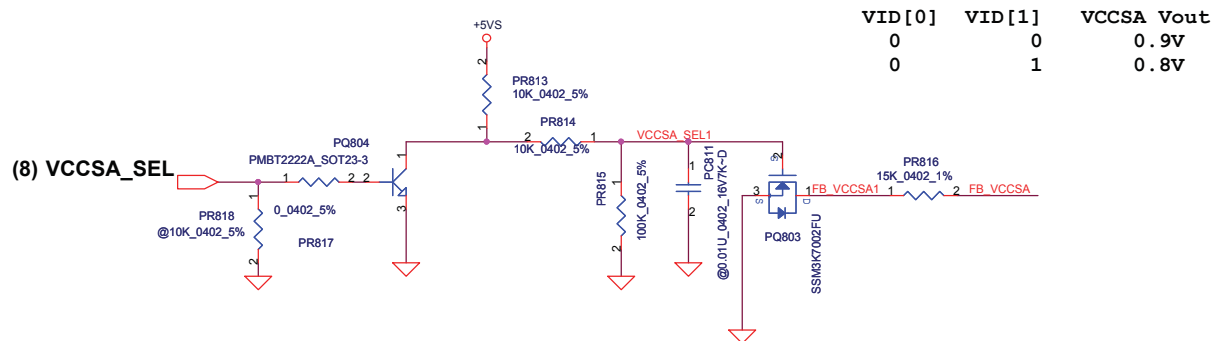
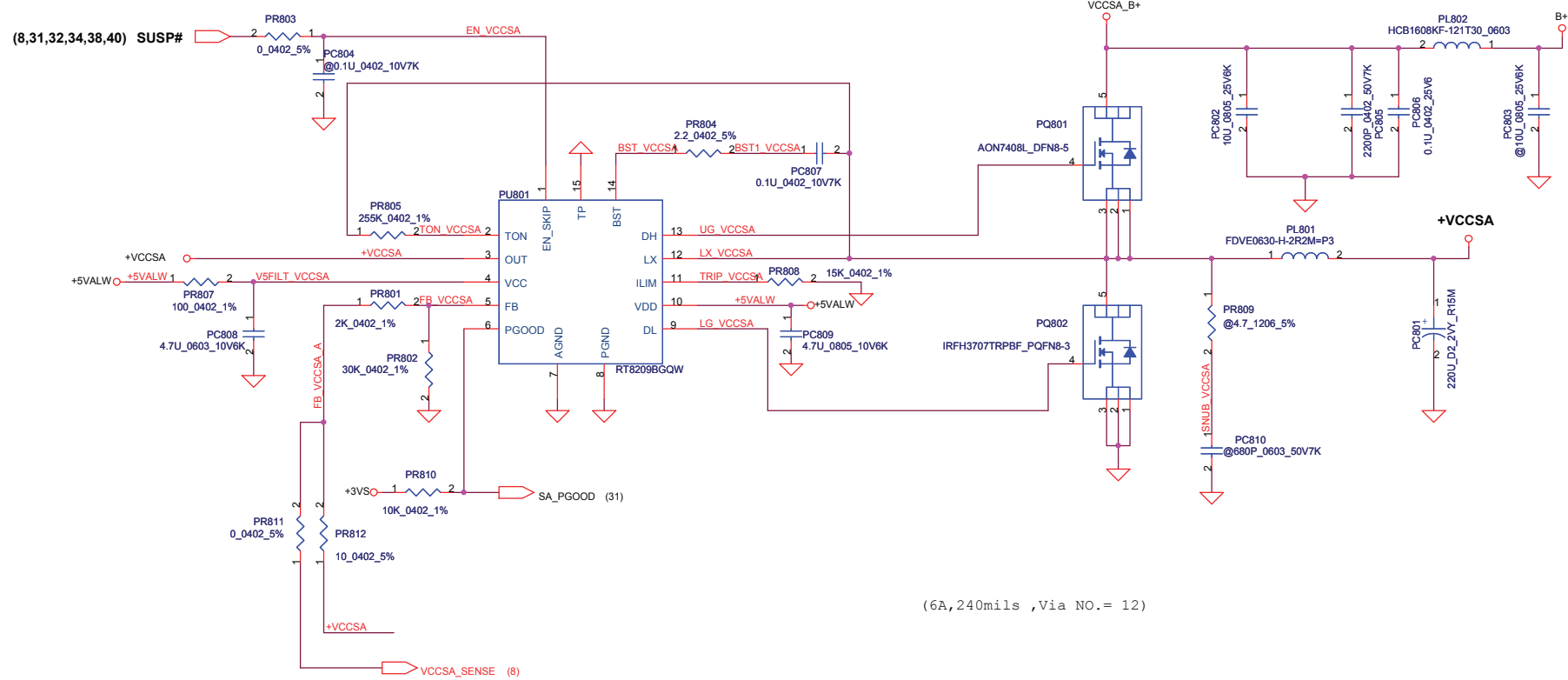




VSSIO_SENSE connect to GND directly.

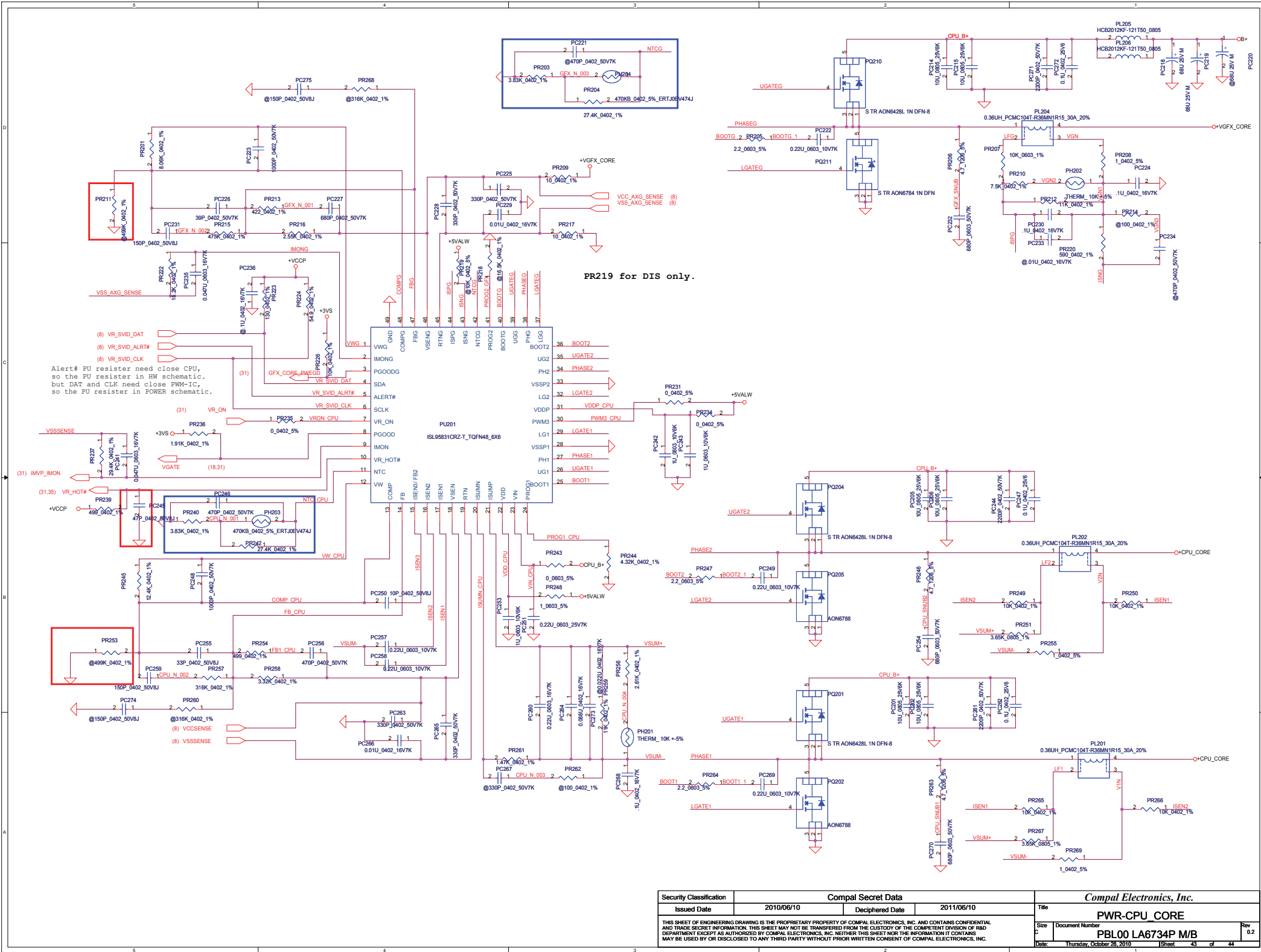
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| VID[0] | VID[1] | VCCSA Vout |
|--------|--------|------------|
| 0 | 0 | 0.9V |
| 0 | 1 | 0.8V |

| | | | | | |
|---|------------|--------------------|------------|----------------------------------|-----------------------------------|
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| | | | | | Date: | Thursday, October 28, 2010 | Sheet |

Revision Change: 0.1 to 0.2

| NO | DATE | PAGE | MODIFICATION LIST | PURPOSE |
|----|-------|----------|---|------------------------------------|
| 1 | 08/12 | All | Remove all components about UMA@ | From UMA/DIS schematic to DIS only |
| 2 | 08/12 | 41 | Change RA16 from 5.1K to 39.2K & connect from SENSE_B to SENSE_A | Headphone out can't detect issue |
| 3 | 08/12 | 46 | Change USB30 from TI to NEC | SPEC request |
| 4 | 08/12 | 27 | Delet U37 and relate schematic. Q16,i connect to HDMI connector directly. R570 from 100K to 20K | HDMI Hot Plug issue |
| 5 | 08/24 | 41 | Change RA9,RA10 to 4.7U | For Audio Precision |
| 6 | 08/24 | 29 | Change CLKREQ_USB30# Pull-hi from +3VS to +3VALW_PCH | Vendor request |
| 7 | 08/25 | 43 | Mount R1368 and C930 | EMI request |
| 8 | 08/25 | 28,29,32 | Change R101,R258, and R1545 to 47ohm | EMI request |
| 9 | 08/25 | 5 | Add R15 between PLT_RST# to U3 | EMI request |
| 10 | 08/25 | 25 | Change C399 to 1U_0603 | EMI request |
| 11 | 08/25 | 45 | Add C760 | EMI request |
| 12 | 08/26 | 10 | Remove C80 | DFB issue |
| 13 | 08/26 | 45 | Change CT31 footprint to B2 | DFB issue |
| 14 | 08/31 | 45 | Add C73,C76,C77, and C761 | EMI issue |
| 15 | 09/01 | 14 | Remove RV33,RV34 | ME issue |
| 16 | 09/02 | 41 | Reserve C931 and R1370 | EMI request |
| 17 | 09/02 | 43 | Remove C208 | EMI request |

Revision Change: 0.2 to 0.3

| NO | DATE | PAGE | MODIFICATION LIST | PURPOSE |
|----|-------|------|-------------------------------|-------------------|
| 1 | 10/08 | 28 | Add R1569 | Power consumption |
| 2 | 10/20 | 43 | Add R725 and pull high +3VALW | For common design |
| 3 | 10/20 | 46 | Remove DT1 | For cost down |
| 4 | 10/20 | 27 | Remove D17 | For cost down |
| 5 | 10/22 | 39 | Reserve D22, D23 | EMI request |

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